Much of the material in chp. 2 is another description of mos transistor concepts from a junior level electronics book like Sedra/Smith.

pg 39, sec. 1.8
....the reason for CMOS dominance is that it is a forgiving technology. CMOS gates are almost guaranteed to function correctly,....the density of processes and the automated CAD available ...systems may be implemented in a highly automated fashion. However, leading edge products (eg. digital ASICS, mixed signal) continue to push the technology...


1. Functional or Logic Behavior – use a Switch model (pmos and nmos) to produce/capture a Netlist.

2. Voltage connections and Energy Flow Behavior – use a transistor diode model to design positioning of source terminals, voltage polarities across nmos & pmos terminals, body effect issues, diode connected transistors, and being able to consider both BJT and MOS devices interchangeably.

3. Speed and Timing Behavior - leads to required values of current; note that more current usually means faster devices that need more power.

Approximate gate delays with either constant current or transistor RC time constants:

I = C*dV/dt for charging and discharging signals. Main discussion starts in section 4.5.

4. A few other performance issues in a digital design are: Power dissipation, size, cost, and various insertion and packaging issues.

5. Reliability and Noise Margin. Although often taken for granted in digital design, the robustness against interference, noise, and component tolerance/degradation is depicted in the inverter DC transfer curve of an inverter. The calculation of the transfer curve for various inverter topologies is a major part of chapter 2, sections 2.3 - 2.5. However, noise margin is not a key performance issue at this stage, so that the main consideration of all the equations in 2.3 - 2.5 will be their applicability to speed and area design issues, which are taken up in later chapters. Both speed and area are greatly influenced by layout decisions, so layout (and thus chip fabrication) is introduced in chapter 3.

Section 2.1.3.1 zero bias Threshold Voltage - this voltage is fixed by the manufacturer, it is not a design decision.
6. Section 2.1.4 Body Effect intro - fig. 2.7 shows a pull down block in a 2 input NAND, relate to section 2.2.2.1 and note calculation on pg. 53 that shows a 0.53v increase in Vth, and that increase in Vth leads to a decrease in current and thus gate speed. This fact is revisited in section 4.5.4.5 (pgs. 223-225), and figure 4.30 shows design issues in a 4 input NAND gate. Note the last paragraph in the section discusses design strategies about which signal should go to which input of the 4 input NAND. These design decisions require considerations of the body effect phenomenon and layout for best timing performance.

7. Pgs. 51 –53. section 2.2.1 Basic DC design equations for a MOS transistor (both types), useful for speed estimates and DC transfer curves. Vgs and Vds voltages determine Linear or triode region vs. Active or saturation region (boundary at Vds = Vgs – Vth). Design decisions will be W/L ratio and desired voltage drops. Beta (B) combines the W/L ratio with uCox (0.5um NMOS typically 100uA/V^2).

8. Section 2.2.3 (MOS models) and section 2.2.4 (Linearized equations – small signal) are useful for paper and pencil calculations of timing in the early design stages.

9. Pgs. 62 – 71. Main ideas and calculations for DC transfer curve and noise margins in a standard CMOS inverter. Describe shift of gate trip voltage with Bn/Bp ratio and other factors, for example: manufacturing tolerance, operating temperature, aging, etc. Although this trip voltage shifting is ok for digital circuits, it is disastrous for analog circuits, and thus analog circuits have to work around it (one strategy is to use feedback and 3 voltage rails vs. 2 voltage rails, Vdd & Vss, in digital circuits).

10. An inverter is the same circuit for digital or analog amplifiers, and is the basic building block for larger scale digital (nand/nor, latches, flip flops, registers & buses...) and larger scale analog (op amps, filters, data converters, RF mixers,...). The main difference is in the design flows (and design decision making) that are used for digital inverters vs. analog inverters.

11. Section 2.4 All inverter circuits are analyzed in a manner similar to that on pgs. 62-71. In general, the noise margins on these circuits are all worse, but other performance factors (speed, layout area) can be better than the standard CMOS inverter, especially for more complex gates and structures.

12. Section 2.5 Differential Inverters are interesting, related to analog design issues, and have better speed and mixed signal performance than standard CMOS inverters.

13. Section 2.6 Transmission Gate is important to understand for switches and muxes and bus considerations. Section 2.7 extends this with Tristate Gates. Note, that tristate topologies are important in Chp. 5 for a wide range of digital blocks, and the VCO project uses a tristate gate with an analog control voltage on the enable inputs (C and –C).