A 256k@32-bit Capture Card for the IIP Radiometer

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Introduction

This document describes a 32-bit capture card for the IIP Radiometer RFI processor described in [1]. The capture card will be capable of capturing 32-bit data at 100MSPS, to a depth of 256k samples (which is equivalent to a capture time of 2.6ms.)

1 Capture Card Interface

The digital part of the radiometer project is broken into several stages of development (Digital IF, APB, FFT, etc) and it is important to be able to capture results from each stage. It is of equal importance that each stage be capable of interfacing to the proceeding stage. Consequently a standard interface was developed using a high density 68-pin SCSI-3 connector. This is the same connector which is used to interface data to the PC using the PCI-DIO-32HS digital acquisition card [2]. A photograph of the capture board is shown in Figure 1, where the male connector (black) is the input to the capture card and the female connector (silver) is the PCI-DIO-32HS interface connector. Each of the radiometer development stages will have a similar connector layout.

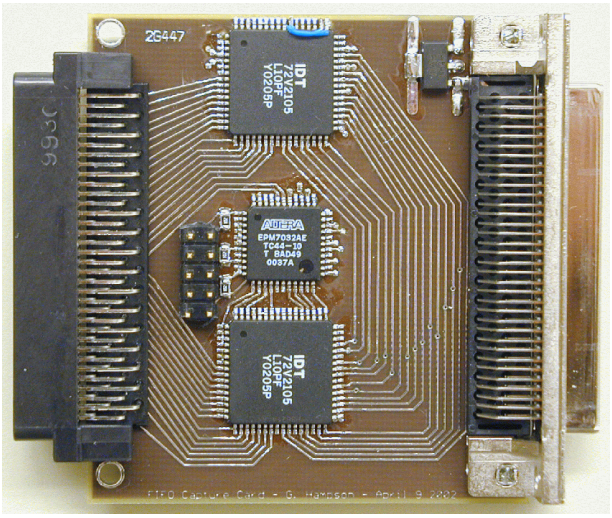


Figure 1: Photograph of the FIFO capture board. Input is via the black male SCSI-3 68-pin connector. Output is via the silver female SCSI-3 68-pin connector. The board consists of two FIFOs and a FPGA controller. (Photo is approximately actual size.)

It was decided that the ADC used (AD9410 [3]) in the radiometer has an output resolution of 10-bits. Allowing for bit growth of fixed point arithmetic in subsequent stages of the radiometer, then an intermediate resolution of 16-bits would be sufficient. This is also an easy number of bits to capture and read into PC memory.

Consequently, the FIFO capture card has two 16-bit inputs (which could be treated as a single 32-bit word if required.) Each stage of the radiometer has two 16-bit inputs and two 16-bit outputs buses. Additionally, there are two control input and two control outputs, which could be clocks, clock enables, etc.. This results in 34 digital I/O signals per connector - and 34 ground pins per connector.

2 Capture Card Implementation

A block diagram of the capture card is shown in Figure 2. The controller is implemented in a Altera EPM7032AETC44-10 (a $2 FPGA) for which the source code is listed in Appendix A. Data is directly written to each FIFO input. The function of `controla` and `controlb` is arbitrary (typically one is a clock and the other a write enable.) If the function of `controla` and `controlb` change then it is necessary to recompile this code and program the FPGA.

The tri-state data outputs of the FIFOs [4] are tied together and each FIFO is selected independently using FIFO output enables. The reset signal from the PCI-DIO-32HS is synchronized to the input clock (`controla` or `controla`) so that one FIFO doesn't start writing before the other. As a result the samples are synchronized and not out of order.

The maximum read clock rate (`pclk`) is 20MHz. The interface pauses occasionally due to the PC card memory flushing. The `ack` signal indicates this and temporarily pauses the FIFO reading. The duty cycle (input to output rates) is approximately 5%.

A schematic and layout created in the Eagle CAD software is shown in Appendix B and Appendix C, respectively.

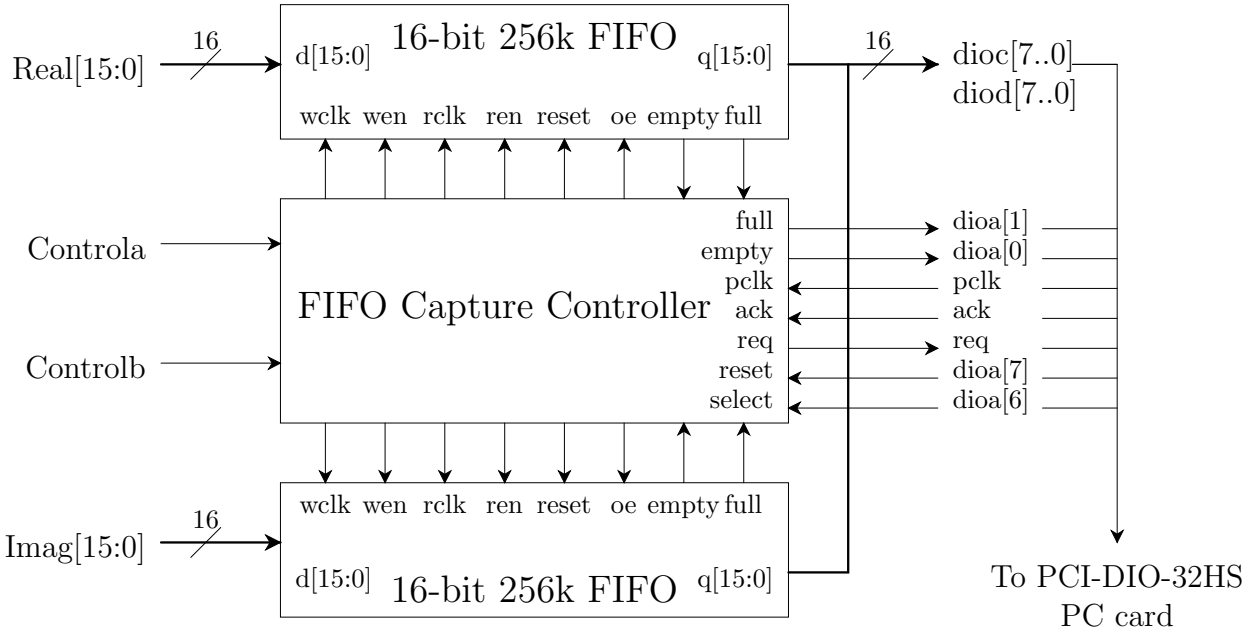


Figure 2: Block diagram of the FIFO capture board.

Summary and Conclusions

This report has presented an implementation of a 32-bit 100 MSPS capture card. The card interfaces to the PCI-DIO-32HS data acquisition card. An approximate input to output duty cycle of at least 5 to 10% can be expected.

The capture card also defines the standard for I/O connections on intermediate stages of the radiometer project. It permits 32-bits of data and 2-control signals to pass between subsequent stages.

Although no results from the capture card have been shown here directly, it has been functioning correctly in current tests.

References

[1] S. W. Ellingson, "Design Concept for the IIP Radiometer RFI Processor," January 23 2002. http://esl.eng.ohio-state.edu/rfse/iip/rfiproc1.pdf.

[2] *High-Speed 32-bit Digital Pattern I/O and Handshaking*, National Instruments, 2002. http://www.ni.com/pdf/products/us/2mhw332-333e.pdf.

[3] *10-bit, 210MSPS A/D Converter, AD9410*, Analog Devices Corporation, October 2000. http://www.analog.com/productSelection/pdf/AD9410_0.pdf.

[4] *IDT72V2105 3.3V High Density CMOS SyperSync FIFO, 262144×18-bit*, Integrated Device Technology, Inc., March 2001. http://www.idt.com/docs/72V2105_DS_52815.pdf.

Appendix A: FIFO Controller AHDL Source

```
-- Interface between Standard Output Connector and PCI-DIO-32HS
-- Grant Hampson 3 May 2002
SUBDESIGN fifocontroller
(
   controla,         -- clock/control bits
   controlb,
   fifo_imag_full,   -- FIFO output signals
   fifo_imag_empty,
   fifo_real_full,
   fifo_real_empty,
   dioa_in[7..6],    -- input signals from PCI-DIO-32HS interface
   pclk,             -- 20MHz clock from PC
   ack1              -- read enable signal
      :INPUT;

   fifo_real_wen,    -- real FIFO controls
   fifo_real_wclk,
   fifo_real_mrs,
   fifo_real_rclk,
   fifo_real_ren,
   fifo_real_oe,
   fifo_imag_wen,    -- imaginary FIFO controls
   fifo_imag_wclk,
   fifo_imag_mrs,
   fifo_imag_rclk,
   fifo_imag_ren,
   fifo_imag_oe,
   dioa_out[1..0],   -- output signals to PCI-DIO-32HS interface
   req1
      :OUTPUT;
)

VARIABLE
   reset_sync : DFF; -- register to synchronise FIFO reset to AD clock edge

BEGIN
   dioa_out[0] = fifo_real_empty OR fifo_imag_empty;
   dioa_out[1] = fifo_real_full OR fifo_imag_full;
   req1 = VCC;-- request to send always
   reset_sync.clk = controlb;                -- synchronise reset to controlb
   reset_sync.d = dioa_in[7];                -- bit 7 resets the FIFO when low
   fifo_real_wen = GND;
   fifo_real_wclk = !controlb;               -- controlb is a clock for real FIFO
   fifo_real_mrs = reset_sync;               -- synchronised reset signal
   fifo_real_rclk = pclk;                    -- read clock from PCI-DIO-32HS
   fifo_real_ren = (!ack1) OR dioa_in[6];    -- stop FIFO reading
   fifo_real_oe = dioa_in[6];                -- bit-6 low selects real output
   fifo_imag_wen = GND;
   fifo_imag_wclk = !controlb;               -- controlb is a clock for imag FIFO
   fifo_imag_mrs = reset_sync;               -- synchronised reset signal
   fifo_imag_rclk = pclk;                    -- read clock from PCI-DIO-32HS
   fifo_imag_ren = (!ack1) OR (!dioa_in[6]); -- stop FIFO reading
   fifo_imag_oe = !dioa_in[6];               -- bit 6 high selects imaginary output
END;
```

Appendix B: FIFO Capture Schematic

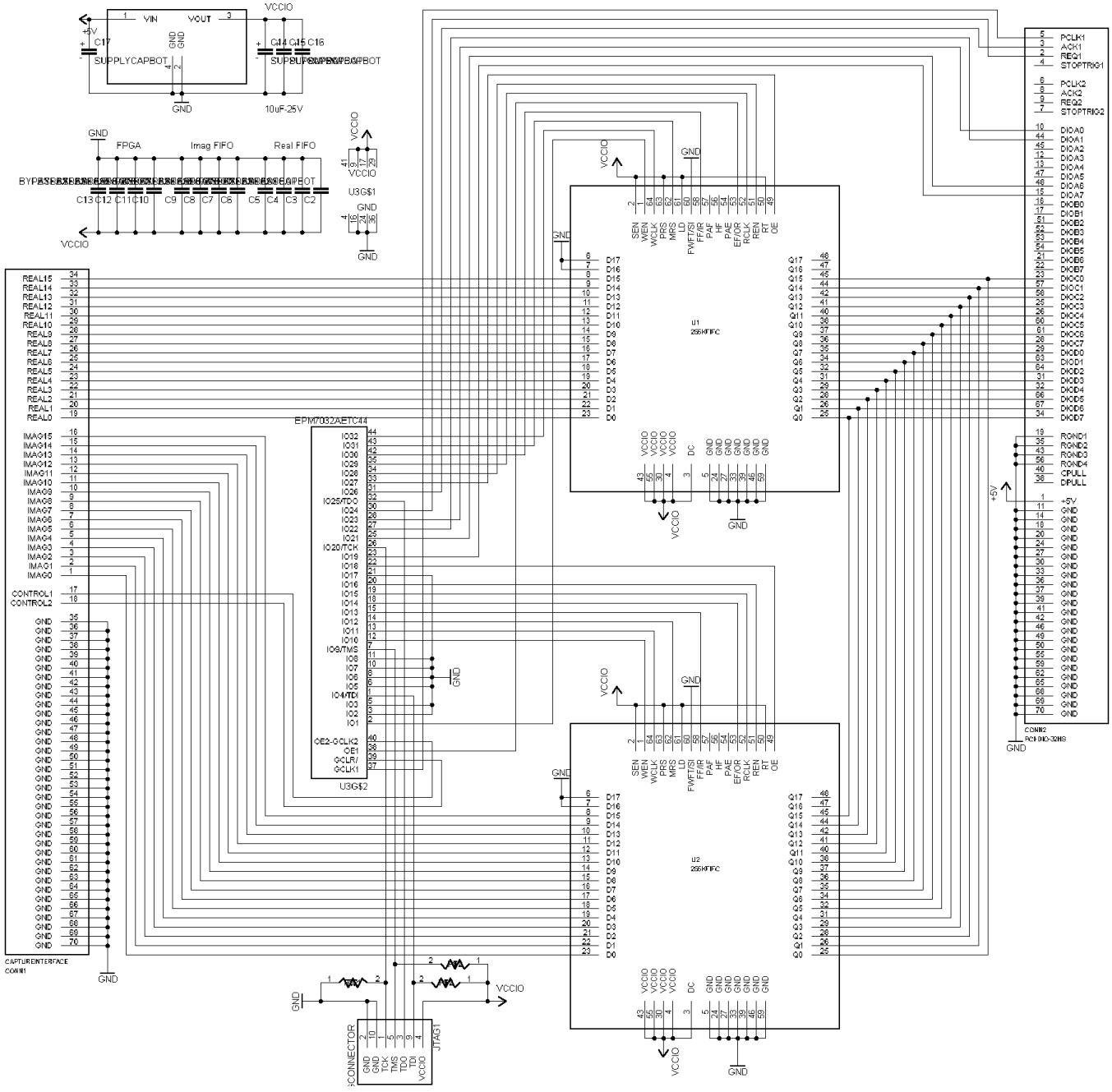
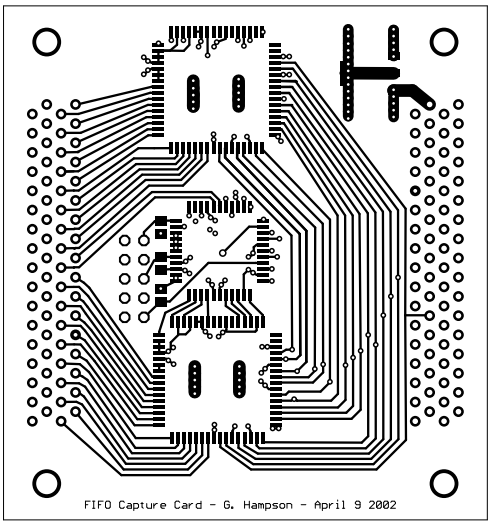
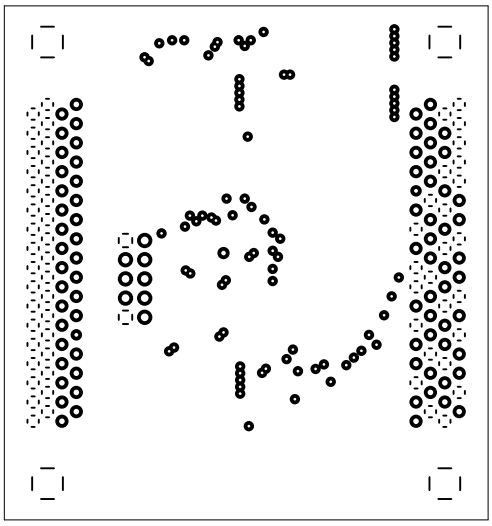


Figure 3: The schematic of the FIFO capture board created using Eagle CAD software (`www.cadsoft.com`). Custom components were created for the input and output connectors, FPGA and FIFOs. Pin numbers indicate actual pin numbers on the components.

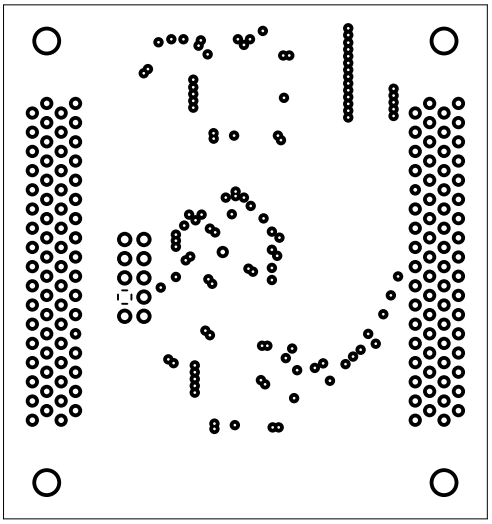
Appendix C: FIFO Capture Layout Plots



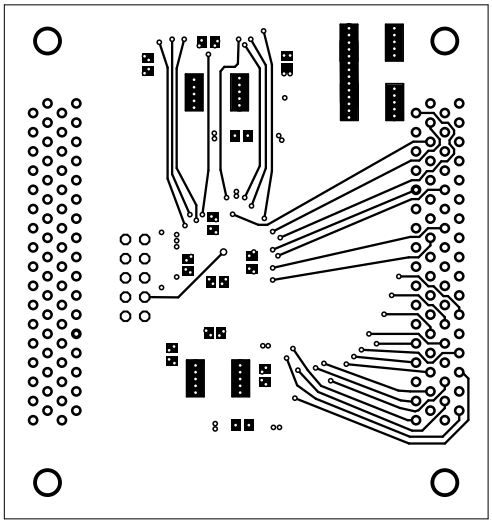
(a) Component Side



(b) Ground Plane



(c) Power Plane



(d) Solder Side

Figure 4: The four layers of the FIFO capture board. This board is manufactured by PCBexpress (`www.pcbexpress.com`) and costs $75. (a) The top layer consists mainly of signal routing. Power (+5V) comes from the PC and is regulated to 3.3V. (b&c) The power and ground plane plots are negative images. (d) The solder side contains power capacitors and some signal connections.