A Possible Dual Digital IF Processor Implementation

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October 1, 2002

Currently, the IIP radiometer Digital IF Processor (DIF) [1] operates on a single IF channel. This document describes a possible upgrade of this system to a custom dual channel digitizer and IF processor. Currently, the digitizer consists of a evaluation board as well as a board containing an Altera FPGA with the DIF processor. The existing architecture is shown in Figure 1. The AD9410 operates in the second Nyquist zone

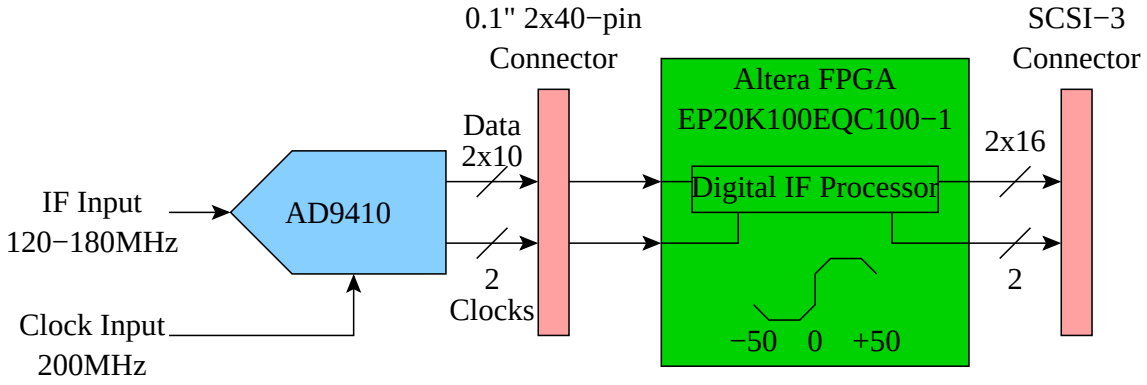

Figure 1: Existing AD9410 evaluation board and DIF board.

with a sampling rate of 200MHz. The input data is shifted down in frequency by 50MHz (FS/4 down) and filtered to remove the image component. The data is then shifted up in frequency by 25MHz (FS/4 up.) The output of the digital IF processor is a 100MHz complex output with slightly less than 50MHz of band width.

1 A Dual Channel Digitizer/DIF Processor

The upgrade path of the digitizer and DIF is to integrate the two functions onto the same PCB. This is illustrated in Figure 2 where each DIF has a different final stage frequency shift (+25MHz and -25MHz.) The DIF processor consumes approximately 86% of the LE in the FPGA. Consequently each DIF processor is implemented in a separate FPGA. It could be possible to use a larger FPGA except that it is desirable to keep the AD9410 data lines as short as possible to reduce loading. There is no economical gain in going to a FPGA double the size. The two complex data paths from the DIF can be added together and output to the single SCSI-3 connector.

Figure 3 is a slightly more detailed layout of the proposed digitizer and DIF board. The IF input of the ADC will remain AC coupled, however the clock input will be changed

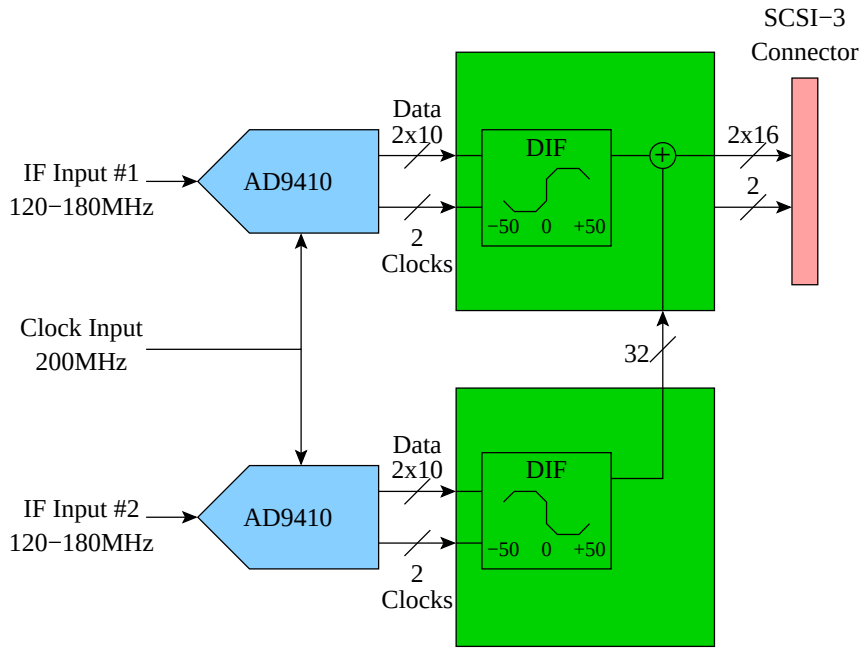

Figure 2: Combined dual channel digitization and DIF board.

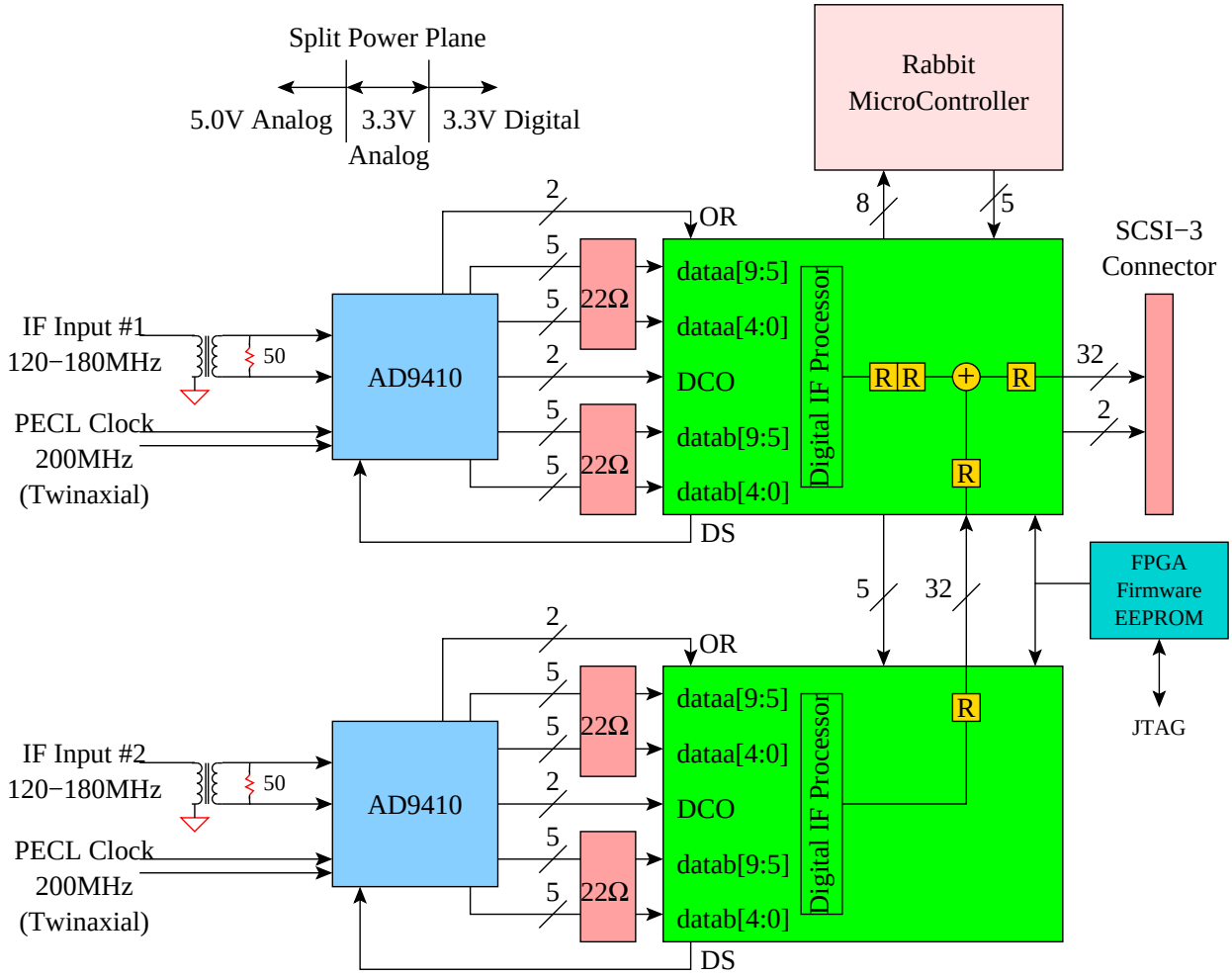

Figure 3: Detailed layout of the proposed digitizer/DIF board.

to a PECL differential input using a twin-axial cable. There are several PECL 200MHz clocks available from Valpey-Fisher [2]. These clocks operate from a 5.0V or 3.3V power supply. A 100ppm device was quoted to be approximately $30. For a 100ppm device the maximum possible frequency error is $100 \times 200 = 20$kHz, which is still a fraction of the FFT bin width (100MHz/1024=98kHz.) The new 200MHz clock module will produce a 10MHz reference clock (divide by 20) for the LO synthesizers.

An important addition to the board is a rabbit microcontroller which will allow control over the output data [3]. The Rabbit is controlled via a TCP/IP link. The different modes which can be selected are: select AD9410 data or ROM test data; select Digital IF data or AD9410 raw data; enable DIF#1 and/or DIF#2 processors. A 4k sample test ROM will be loadable via the Rabbit.

In addition to controlling the dual-DIF, it will also possible to monitor the OVER-RANGE output of the AD9410. The over-range output will presented as counts per second. This may provide some feedback to the RF front-end gain control setting.

The two AD9410 converters also need to be synchronized to an appropriate state using the DS input of the AD. It is believed this will be a direct feedback of the DCO output, but this is not made particularly clear in the data sheet [4].

The AD9410 requires three separate power planes to operate: 5.0V analog, 3.3V analog and 3.3V digital. A similar layout to the evaluation board will be used. The ground plane is solid beneath (and around) the AD9410. Analog power regulation (linear) will be external to the board since it is almost four watts of power.

Finally, there will be several status LEDs to indicate power, mode, over range, etc.. The Altera FPGA will also have a EEPROM which contains the FPGA's firmware. The FPGA will automatically program itself upon power up.

2 Summary and Conclusions

This report has presented a brief overview of the possible requirements and features of a dual channel digitizer/DIF processor board. The new board contains many features that will help with debugging and monitoring. A majority of the work required will be in the drawing of the new schematic/layout. The board can be constructed one channel at a time to confirm the required ADC performance.

References

[1] G. A. Hampson, "An FPGA Implementation of the Digital IF Processor," March 7 2002. http://esl.eng.ohio-state.edu/~swe/iip/digitalif.pdf.

[2] *VF561 PECL Compatible Surface Mount Clock Oscillator*, Valpey-Fisher. http://www.valpeyfisher.com/Data/DescriptionFiles/VF(F0314).pdf.

[3] *RCM2200 RabbitCore*, Rabbit Semiconductor. http://www.rabbitsemiconductor.com/products/rcm2200/index.html.

[4] *AD9410, 10-bit, 210MSPS A/D Converter*, Analog Devices Corporation, October 2000. http://www.analog.com/productSelection/pdf/AD9410_0.pdf.