Software-Defined Radar for MIMO and Adaptive Waveform Applications

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***Abstract*— The development of a software-defined radar testbed is described. The testbed is to be used to explore advanced techniques such as multiple-input multiple-output radar and adaptive waveforms. The system features a fully programmable, dual-channel, arbitrary pulsed waveform generator with a quadrature downconverting receiver. The system can generate waveforms of up to 500 MHz instantaneous bandwidth at a center frequency tunable from 2-18 GHz. The RF front end features two independent transmit and receive channels that can be multiplexed between four dual-polarized transmit and four dual-polarized receive antennas.**

I. Introduction

The advancement of high speed digital technology is enabling the exploration of several new radar techniques, including multiple-input multiple-output (MIMO) operations and the use of adaptive waveforms. MIMO radar uses spatially diverse transmitters and receivers to overcome target fading effects [1], [2] or to estimate a target's location with high resolution [3], [4]. Waveform adapation is used to match the transmitted waveform to the target's impulse response in order to improve target detection and to aid in target identification [5], [6]. Both techniques have unique requirements that are not typically met by traditional radar systems, making it difficult to study performance in real-world scenarios.

The evaluation of MIMO and adaptive waveform techniques is greatly simplified through the use of a flexible radar development platform. An implementation of such a platform (called the software-defined radar (SDR) in what follows) that provides a highly reconfigurable, multi-channel, low-power radar testbed is described in this paper. The radar hardware consists of three distinct sections: a commercially available high speed digital processing system operating at 1 giga-sample per second (1 GSPS), a custom multi-channel RF up/downconverter with 500 MHz of instantaneous bandwidth and a center frequency tunable from 2-18 GHz, and a switch matrix which multiplexes two transmit and receive channels among an array of antennas. Details of the digital and RF hardware are discussed in Section II, while Section III describes the software framework being developed to implement standard radar functions. Some preliminary measurements were made to demonstrate the potential range and Doppler resolution of the system and the results are discussed in Section IV.

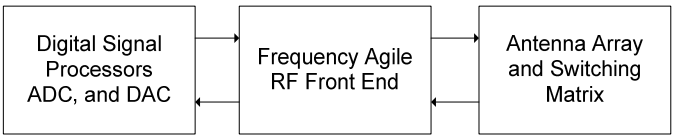

Fig. 1. Overview of the softare-defined radar.

II. Hardware

An overview of the SDR system is given in Figure 1, which outlines three main components: the digital back end that includes the digital-to-analog (DAC) and analog-to-digital (ADC) converters and associated digital signal processing (DSP) components, the frequency-agile RF front end, and the antenna array and switching network. The following sections discuss these components in turn.

A. Digital Back End

The SDR is based on a modular digital signal processing platform whose components are commercially available from *Sundance Multiprocessor Technology Ltd.*. A block diagram of the complete platform is given in Figure 2. The *Sundance* part numbers of individual modules are given in parenthesis in the figure, and additional information on each of these modules can be found in reference [7]. The system consists of two PCI carrier cards that are housed in a standard PC.

The first PCI carrier card holds two quad-DSP modules (SMT395Q), providing the system with an array of eight Texas Instruments TMS320C6416T DSPs. These are 32-bit fixed-point DSPs that operate at a 1 GHz clock rate. In addition, each quad-DSP module contains a Xilinx Virtex-II Pro field-programmable gate array (FPGA). These FPGAs implement the fabric required for intercommunication between each of the four processors on a given module. For communication between modules, each quad-DSP module also contains a set a high-speed data bus connections. These can be used to connect the two DSP modules to each other or to modules located on the second PCI carrier card as indicated in the figure.

The second PCI carrier card houses the ADC and DAC modules. Both the ADC and DAC are dual-channel devices operating at 1 GSPS for each channel, providing effectively 500 MHz of instantaneous bandwidth in each channel. The DAC is a 14-bit device, while the ADC is an 8-bit device.

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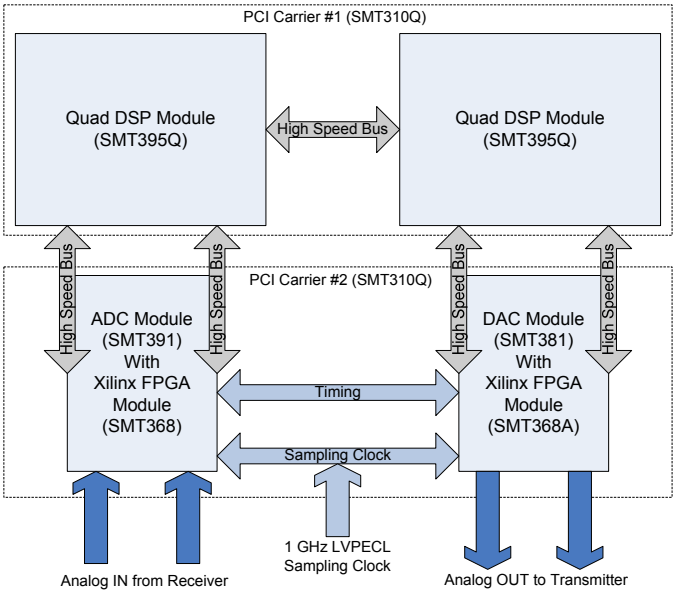

Fig. 2. The SDR digital back end consists of two PCI carrier cards. The first carrier card is dedicated to signal processing, while the second holds ADC and DAC modules with their associated FPGAs.

Since these devices produce data at an extremely high rate, each is attached to its own FPGA module. These FPGA modules (both the SMT368 and SMT368A as shown in Figure 2) utilize Xilinx Virtex-4 SX35 FPGAs to implement the digital interface to the DAC and ADC. In addition, these FPGAs control high speed data buses that connect to the DSP modules housed on the first PCI carrier. On the transmit side, the two data buses are used to transfer samples of the transmit waveforms for each channel from the DSPs where they are generated to the DAC. On the receive side, the two buses transfer independent channels of sampled data from the ADC to the DSPs for further processing. An additional digital connection between the FPGAs is used to maintain transmit and receive timing.

For fully coherent operation, the phase between the ADC and DAC sampling clocks must be constant. To achieve this, a low-voltage positive emitter-coupled logic (LVPECL) differential clock is generated using a bench source and passed to both the ADC and DAC. The ADC divides this clock by a factor of four and provides this new 250 MHz clock to its associated FPGA. The DAC similarly divides the 1 GHz clock by two and provides a 500 MHz clock to its FPGA. The FPGAs then further divide these clocks internally to support various stages of processing that will be described in section III.

B. RF Front End

The SDR employs a frequency-agile RF front end to tune 500 MHz of instantaneous bandwidth to a center frequency located anywhere from 2 to 18 GHz. Since the SDR system is primarily a short range low power radar testbed, the design of the RF front end is significantly simplified by removing the need for extensive receiver protection and high-power

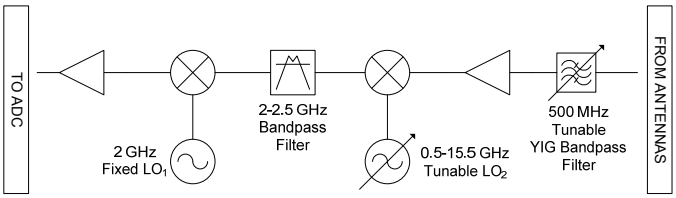

Fig. 3. Simplified diagram of the tunable 2-18 GHz SDR receive channel.

amplifiers and switches. Because of this, the transmit and receive channels are very similar, and only the receive channels will be analyzed here with the understanding that the transmit channels will be nearly identical in reverse.

A simplified block diagram of one channel of the SDR receiver is illustrated in Figure 3. The receiver is based on a standard superheterodyne design with two local oscillators (LO). The first LO is fixed at 2 GHz, and the corresponding anti-aliasing filter is a fixed bandpass filter from 2-2.5 GHz. This filter is not required to tune, and has sharp transition regions. The second LO is tunable from 500 MHz to 15.5 GHz in order to downconvert any incoming signal from 2-18 GHz to the appropriate intermediate frequency. To avoid aliasing, the second filter must also be tunable. Current state-of-the-art bandpass yttrium iron garnet (YIG) filters with 500 MHz bandwidth can only be tuned from 6-18 GHz. Therefore, switches are used to select either the tunable YIG filter or any one of a series of fixed 500 MHz bandpass filters which cover the 2-6 GHz band in discrete steps.

C. Antenna Switch Matrix

MIMO radar is a potential application of the SDR testbed so multiple independent transmit and receive channels are desirable. The digital and RF sections discussed previously implement two independent transmit and two independent receive channels that can be configured to operate as a 2-by-2 MIMO system. To increase the number of channels by replicating hardware would be straightforward but expensive. As a compromise, an RF switch matrix is used to expand the number of transmit and receive antennas to 4-by-4.

Figure 4 outlines the switch layout on the transmit side. Each transmit channel is fed to a four-port switch that selects a specific antenna. A corresponding two-port switch on the desired antenna selects between these two possible inputs, and a second switch in series selects the polarization of the antenna. In this manner, either transmit channel can be connected to the desired polarization on any of four antennas. This configuration prevents two transmit channels from being connected to the same antenna, as for example in simultaneous polarimetry; however the time delays required to switch between polarizations were not deemed prohibitive. The four transmit antennas in Figure 4 are separate from the four receive antennas, so it is also not intended to transmit and receive on the same antenna.

Figure 5 outlines the receive side switch matrix and antennas. The antennas' output ports for each polarization are inputs to a polarization selecting switch. The output of this switch is

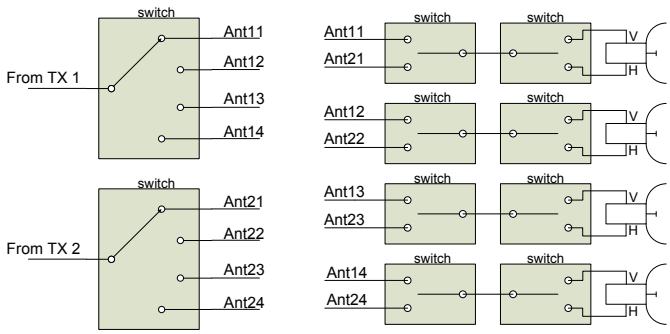

Fig. 4. The transmit switch matrix enables two transmit channels to be switched among four dual-polarized antennas.

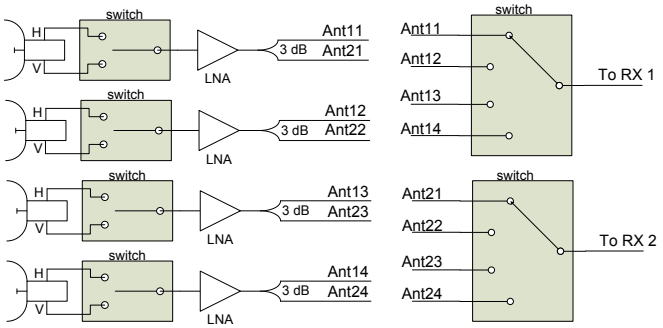

Fig. 5. The receive switch matrix connects four dual-polarized antennas to two receive channels, and includes LNAs at the antennas to mitigate the effects of long, lossy cables.

then connected to a low-noise amplifier (LNA) whose output is then passed to a power divider. The outputs of all four power dividers are connected to two four-port switches corresponding to the two receive channels. Since it is likely that the antennas will be connected to the rest of the RF system by long cables, including LNA components close to the antennas reduces the impact of cable loss on the receiver's overall noise figure.

Antennas suitable for use with the SDR system are currently being reviewed. It is likely that the choice of antennas will be determined by the particular application being studied. For example, MIMO systems typically require a very wide beamwidth, while it may be desirable to have a more traditional narrow-beam antenna for adaptive waveform applications. MIMO applications also motivate larger spatial separations among the transmit and receive antennas.

III. Software

The SDR digital back end outlined in section II-A is an extremely flexible data processing system. A basic framework has been designed to implement an arbitrary pulsed waveform generator (APWG) and receiver that can coherently transmit and receive pulsed waveforms with bandwidths up to 500 MHz. This framework primarily uses resources available in the FPGAs connected to the ADC and DAC modules, leaving the DSPs largely free to perform higher-level functionality such as MIMO or adaptive waveform processing. First, the

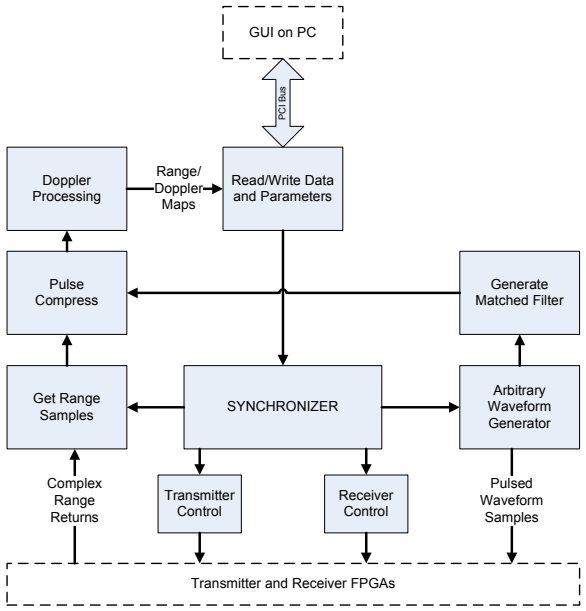

Fig. 6. Flowchart showing the SDR software running on network of eight digital signal processors.

software running on the DSPs will be discussed, followed by a description of the software running on the FPGAs.

The SDR software is controlled by a graphical user interface (GUI) which runs on the user's PC. The GUI provides a simple interface for the user to control the radar and to view the output of the SDR system in real-time. The GUI communicates with the SDR software by passing messages back and forth over the computer's PCI bus to one of the DSPs. This connection is shown at the top of Figure 6. The various functions performed by the DSPs can be compartmentalized into tasks, and each task has its own block in the figure. The "Read/Write Data and Parameters" task is responsible for implementing this interface over the PCI bus. The "Synchronizer" task ultimately receives the user control and is responsible for setting up the transmitter and receiver FPGAs which will be discussed next. Additionally, the Synchronizer task signals the "Arbitrary Waveform Generator" task to create the waveform to be transmitted along with the corresponding matched filter. Another task is dedicated to buffering the complex range returns which are transferred from the receiver FPGA over a high-speed bus discussed earlier when triggered by the Synchronizer. The complex range returns from multiple transmit pulses are pulse compressed following the standard procedure outlined in [8] with the appropriate matched filter. Fast Fourier transforms (FFT) are then computed for each range bin, and the results are passed to the GUI for display or further processing.

A diagram of the software running the the FPGAs for one transmit and one receive channel is illustrated in Figure 7. The framework is replicated in the actual system to support two transmit and two receive channels. As described earlier, the DSPs are used to generate samples of an arbitrary pulse, and these samples are transferred over a high speed bus (shown in Figure 2) to the waveform memory in the transmit

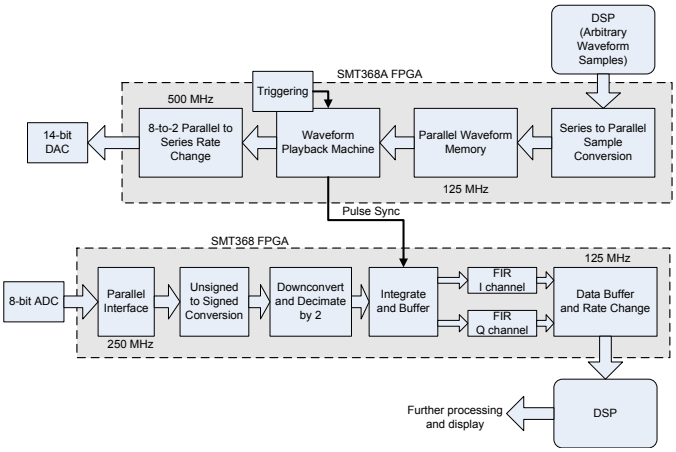

Fig. 7. Flowchart showing the FPGA transmitter and receiver software running on the SMT368A (transmit) and SMT368 (receive) FPGAs.

FPGA (SMT368A). A programmable triggering mechanism configured by the DSPs controls when the pulse data is sent to the DAC for playback. Because the playback occurs at a clock rate of 1 GSPS, the FPGA stores the waveform in sets of eight samples in parallel so that the memory in the FPGA is only clocked at 125 MHz, well within the operating clock frequency of the FPGA. This scheme requires a series of serial-to-parallel and parallel-to-series conversions however, before and after the memory respectively. The pulse samples are transferred to the DAC two at a time at a clock rate of 500 MHz. The DAC then reorders the parallel samples internally and plays them in series.

The interface between the ADC and the receive FPGA (SMT368) operates at 250 MHz, such that four samples of the received signal are transferred out of the ADC in parallel on every clock cycle, for each channel. This parallel data is converted from unsigned to signed binary representation and then buffered. This buffering stage is capable of coherently integrating up to 256 pulse returns which consist of up to 2048 samples each. Both of these parameters can be tuned on a pulse-to-pulse basis. The data is then reordered and converted from parallel to series format as it leaves the integrate and buffer stage and is passed through two finite impulse response (FIR) filters. The net result of the reordering and filtering of the data is the creation of in-phase and quadrature components through a process similar to that outlined in Figure 1 of reference [9]. This in-phase and quadrature data is then buffered again before being transferred back to the DSP modules over a high speed bus.

The timing and length of the transmit pulses are fully parameterized and can be configured by the DSPs without reprogramming the FPGAs. An overview of the pulse parameters and pulse timing is provided in Figure 8. Once a waveform has been transferred to the transmit FPGA for playback, the triggering block in Figure 7 controls two effective PRFs: slow and fast. The fast PRF controls the the timing of pulses that are to be coherently integrated. This is typically done as fast as possible, and therefore is ultimately determined by the sum

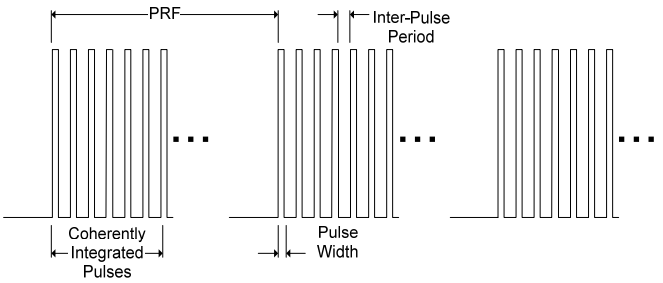

Fig. 8. The pulse parameters (pulse length, IPP length, number of pulses integrated, fast and slow PRFs) are fully configurable by the DSPs.

of the pulse width and the inter-pulse period (IPP). A slower PRF controls the rate at which the sets of coherently integrated pulses occur, and the rate at which the coherent integration results are transferred to the DSPS. This slow PRF is important for any subsequent Doppler processing.

IV. Measurements

The RF front end outlined in Section II-B has not been fully completed. In the interim, a simple prototype RF front end operating with a fixed 6 GHz center frequency is being used to test the digital back end and associated software. As a simple test, the SDR was configured to transmit a 500 MHz linear FM (chirp) waveform with a pulse length of 800 ns. 90 coherent integrations were performed for each pulse and 128 pulse returns were recorded. The fast PRF was 150 kHz, while the slow PRF was 1.5 kHz. A measurement was made in a parking lot with a small pickup truck (Chevrolet S-10 with a total length of approximately 4 m) traveling away from the radar. The 128 radar returns were each pulse-compressed and 256-point fast Fourier transforms (FFT) were computed for each set of 128 samples at a given range gate.

The resulting range-Doppler map in dB is shown in Figure 9. Since the radar was stationary when the measurement was made, other stationary targets and clutter appear in a vertical line with zero velocity (center). The truck, moving away from the radar at approximately 8 m/s, appears as a distinct target with negative velocity (left of center). The truck also appears as a small target with a positive velocity (right of center), which is primarily due to inadequate image rejection in the prototype RF front end. One of the primary features of the SDR is the ability to transmit and receive waveforms with instantaneous bandwidths up to 500 MHz. This results in a range resolution of approximately 1/3 m, so individual scattering centers on the truck are clearly visible. For example, the strongest scatterer is likely the corner formed by the truck bed and the back of the cab. This is clearly visible in the figure and is distinguishable from other scatterers towards the front and rear bumpers of the truck.

V. Conclusion

The SDR is being developed to provide a reconfigurable, highly flexible radar system for testing MIMO and adaptive waveform techniques. It is based on a commercially available

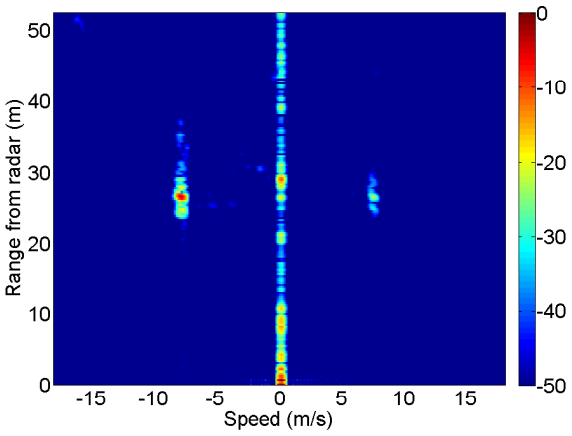

Fig. 9. Range-Doppler map of a small pickup truck moving away from the radar at approximately 8 m/s. The x-axis represents velocity, with positive numbers indicating opening velocities and negative numbers indicating closing velocities. The y-axis indicates range from the radar.

digital back end that provides dual-channel ADC and DAC components operating at 1 GSPS and significant signal processing resources. A custom RF front end is being developed with a tunable center frequency from 2-18 GHz, an instantaneous bandwidth of 500 MHz, and a switch matrix/antenna array to expand the two-by-two system to four transmit and four receive antennas. Finally, a radar framework has been developed in software to implement a fully configurable APWG and receiver. Most signal processing resources remain available for implementing higher-level MIMO or adaptive waveform functionality. Preliminary measurements using the digital back end and a prototype RF front end show excellent range and Doppler resolution.

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