Project Step 1
Due Friday Apr 4th

A 4-to-1 mux.
The Unit to Model – A 4-to-1 Mux

- Truth Table

This Unit Can perform any of the logic functions of 2 inputs
Project Step 1

- Objective – Model the unit. Connect the data inputs, A and B, to the Select inputs, the G inputs to the corresponding data lines.

- You will then have a “generic” logic unit that can perform any of the functions of two inputs.
The 16 functions

<table>
<thead>
<tr>
<th>G3 G2 G1 G0</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>zero</td>
</tr>
<tr>
<td>1</td>
<td>NOR</td>
</tr>
<tr>
<td>2</td>
<td>A’B</td>
</tr>
<tr>
<td>3</td>
<td>A’</td>
</tr>
<tr>
<td>4</td>
<td>AB’</td>
</tr>
<tr>
<td>5</td>
<td>B’</td>
</tr>
<tr>
<td>6</td>
<td>XOR</td>
</tr>
<tr>
<td>7</td>
<td>NAND</td>
</tr>
<tr>
<td>8</td>
<td>AND</td>
</tr>
<tr>
<td>9</td>
<td>XNOR</td>
</tr>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>B</td>
<td>A’ + B</td>
</tr>
<tr>
<td>C</td>
<td>A</td>
</tr>
<tr>
<td>D</td>
<td>A + B’</td>
</tr>
<tr>
<td>E</td>
<td>OR</td>
</tr>
<tr>
<td>F</td>
<td>one</td>
</tr>
</tbody>
</table>

*Note that the G values are Hex*
How to model

- Model using a dataflow style
  - Concurrent signal assignment statement
    - \( Y \leftarrow (A \text{ AND } B \text{ OR } C) \text{ NOR } D; \)
  - Conditional signal assignment statement (pp 207-209)
    - \( Y \leftarrow '1' \text{ WHEN } Q = "000" \text{ ELSE } A \text{ AND } C \text{ WHEN } Q = "001" \text{ ELSE } \ldots \)
  - Selected signal assignment statement (pp 272-275)
    - WITH bit_vector_signal SELECT
      - \( Y \leftarrow '0' \text{ WHEN } "0000" \)
      - \( '1' \text{ WHEN } "0010" \text{ OR } "0011" \)
      - \( A \text{ WHEN OTHERS}; \)

- Note that all three of these are concurrent statements of the language.
The testbench

- In this assignment you are given the testbench which will stimulate your model by applying exhaustive testing.
- Copy the file pr_step1.vhdl
  - FROM the web page or from ~degroat/ee762_assign
- The ENTITY is provided for you. Enter the architecture.
Simulate and get results

- Compile the file
- Simulate the design – generate both waveform and a listing of the results.
- Turn in
  - Copy of the code
  - Copy of the listing file
  - Copy of the waveform. BE SURE TO GET THE ENTIRE SIMULATION. Use zoom as appropriate. You will need to simulate for 5200 ns to run all the test cases.