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The authors report the growth by rf-plasma assisted molecular beam epitaxy of AlN/GaN/AlN resonant tunneling diodes which exhibit stable, repeatable, and hysteresis-free negative differential resistance (NDR) at room temperature for more than 1000 bias sweeps between −2.5 and +5.5 V. The device layers were grown on freestanding, Ga-polar GaN substrates grown by hydride vapor phase epitaxy and having a density of threading dislocations between 10^6 and $10^7\,cm^{-2}$. The authors speculate that the repeatable NDR is facilitated by the low-dislocation density substrates. [http://dx.doi.org/10.1116/1.4977779]

I. INTRODUCTION

The high frequency operation of resonant tunneling diodes (RTDs) is possible due to the shorter time scales associated with tunneling in comparison to drift and diffusion, as well as to unipolar transport, which results in minimal minority carrier charging capacitances. Oscillation frequencies of 712 GHz have been observed in InAs/AlSb RTDs,[1] while InGaAs/AlAs RTDs oscillating at 1.1 and 1.9 THz have been reported.[2,3] Gallium nitride-based resonant tunneling diodes are of interest, as the large band offsets between AlN and GaN may enable both high output power and high temperature operation, and recent work by Quispe *et al*. suggest that gating GaN high electron mobility transistors with GaN RTDs may result in associated power gains in excess of 40 dB at terahertz frequencies.[4] A signature of resonant tunneling is negative differential resistance (NDR), which arises under certain bias conditions when the quasi-bound energy states in the quantum well align and misalign with the Fermi level in the injector region as the external bias changes. However, while repeatable NDR has been observed from GaN-based RTDs at low temperature,[5] stable, room-temperature NDR in III-nitride RTDs has proven elusive, especially in devices grown on *c*-oriented substrates.[6,7] We report here on the growth of an AlN/GaN/AlN resonant tunneling diode by plasma-assisted molecular beam epitaxy (MBE) that exhibits repeatable, stable, and hysteresis-free NDR at room temperature over more than 1000 current–voltage sweeps.

II. EXPERIMENT

The RTD structure was grown by rf-plasma assisted MBE on an $18 \times 18\,mm^2$ freestanding, Ga-polar (0001) GaN substrate from Kyma Technologies. The GaN substrate was grown by hydride vapor phase epitaxy (HVPE), and the Ga-polar (0001) surface of the wafer was finished with a chemical–mechanical polish. The threading dislocation (TD) density of the GaN wafer was estimated to be between 10^6 and $10^7\,cm^{-2}$; electron channeling contrast imaging revealed a TD density of $4 \times 10^6\,cm^{-2}$ in a similar wafer from the same vendor.[8]

The HVPE GaN wafer was cleaned prior to loading in the ultrahigh vacuum (UHV) MBE system using a wet chemical procedure starting with a solvent degrease and followed by acid and base etches, which is more fully described elsewhere.[9,10] This *ex situ* cleaning procedure has been shown to reliably result in homoepitaxial GaN layers and devices in which the regrowth interface with the freestanding GaN substrate is not visible when analyzed by cross-sectional transmission electron microscopy (TEM), and no TDs are observed to be generated from that interface.[10,11] Proper cleaning of the freestanding GaN substrate arguably is the most important component of growth, as it prevents the formation of extended defects which can act as leakage paths in the device. After loading into the MBE system, the substrate

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wafer was outgassed under UHV conditions in the preparation chamber for 30 min at 600 °C, and then transferred to the deposition chamber for growth.

The deposition chamber was equipped with dual-filament effusion cells for evaporation of elemental aluminum and gallium; a medium-high temperature, single-filament effusion cell for evaporation of elemental silicon; and an rf plasma source for delivery of active nitrogen. The substrate temperature was measured by a thermocouple mounted behind the substrate and was maintained at a constant temperature of 860 °C throughout the growth.

The design of the layer stack was modeled using a nonequilibrium Green's function formalism, and was optimized to improve resonant tunneling transmission by decreasing the polarization-induced collector barrier. This process included a trade-off between the thickness of the unintentionally-doped (UID) collector spacer and the doping level of the top contact. As shown in Fig. 1(a), the collector barrier can be greatly reduced by increasing the doping concentration in the top contact layer. The layer structure chosen for this investigation is shown in Fig. 1(b). Since crack-free AlN layers can be grown on homoepitaxial GaN layers on low dislocation-density GaN substrates up to a thickness of 4.5 nm,[9] 2 nm-thick AlN barriers were used instead of AlGaN to eliminate potential random alloy fluctuations in the barriers which may result in leakage currents due to percolation-based transport.[12]

The plasma was operated at a constant power and N_2 gas flow of 300 W and 0.9 standard cubic centimeters per minute, respectively. The gallium and aluminum fluxes were chosen to result in N-limited growth conditions with no accumulation of excess metal and a growth rate of 3 nm/min. The silicon effusion cell conditions were chosen to result in a silicon concentration of $5 \times 10^{19}\,\mathrm{cm}^{-3}$ in the GaN buffer (lower contact) and $8 \times 10^{19}\,\mathrm{cm}^{-3}$ in the upper GaN contact layer.

Growth was initiated with a 2-min exposure of the substrate surface to the N plasma, followed by simultaneous opening of the Ga and Si shutters. All layers were grown continuously and without interrupts. Growth terminated with the closing of all shutters, extinguishing the N plasma, and cooling the sample in the MBE system.

Upon removal from the MBE system, the sample was characterized by optical microscopy and atomic force microscopy (AFM). Cross-sectional TEM was also performed on a similarly grown structure to assess the quality of the homoepitaxial layers.

RTDs were then fabricated using optical lithography and liftoff. Ti/Al/Ni/Au and Ti/Al/Ni/Au/Ti metal stacks deposited by e-beam evaporation formed the ohmic contacts to the top and bottom GaN:Si contact layers, respectively. Mesa definition was accomplished using a chlorine-based inductively coupled plasma reactive-ion-etch (ICP-RIE) process. The authors have previously shown that chlorine is present at elevated concentrations in the subsurface GaN which has been etched with a chlorine-based ICP-RIE process,[10] but there are no indications as yet of any effect on device performance. A 300-nm-thick passivation layer of SiO_2 was then deposited by plasma-enhanced chemical vapor deposition. Sidewall treatment and passivation were utilized to suppress any potential surface leakage pathways, thereby minimizing the valley current. Current versus voltage (I-V) measurements were performed at room temperature on more than 50 devices across the wafer. Further details of device fabrication and testing may be found in a previous publication.[13]

III. RESULTS AND DISCUSSION

Optical microscopy of the as-grown surface indicated there were no droplets of excess Ga present. AFM revealed a surface with clear atomic steps punctuated by pits as deep as 40–50 nm, as shown in Fig. 2(a). Roughness analysis over the $5 \times 5\ \mu\mathrm{m}^2$ field of view indicated a z-range of approximately 60 nm and a root-mean-square (rms) roughness of 4 nm. The simultaneous appearance of surface pits and atomic steps, and the apparent lack of correlation of the step edges with the shape or location of the pits, suggest that the pits were formed at or near the end of growth. The surface morphology of similar samples, which were grown using the same Ga flux and substrate temperature but lower Si doping concentrations, are much smoother. Figure 2(b) is an AFM image from one such sample, for which the Si concentration in the upper contact layer was $1 \times 10^{19}\,\mathrm{cm}^{-3}$ except for the

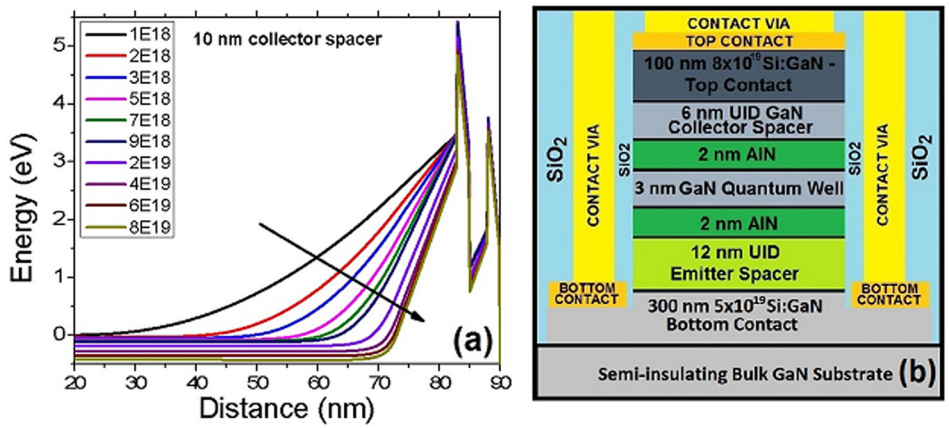

FIG. 1. (Color online) (a) Conduction band energy vs depth for various doping levels, illustrating the narrowing of the collector barrier as the n-type doping concentration increases from 10^{18} to $8 \times 10^{19}\ \mathrm{cm}^{-3}$. The thickness of the UID collector spacer is assumed to be 10 nm. (b) Diagram of RTD layer structure.

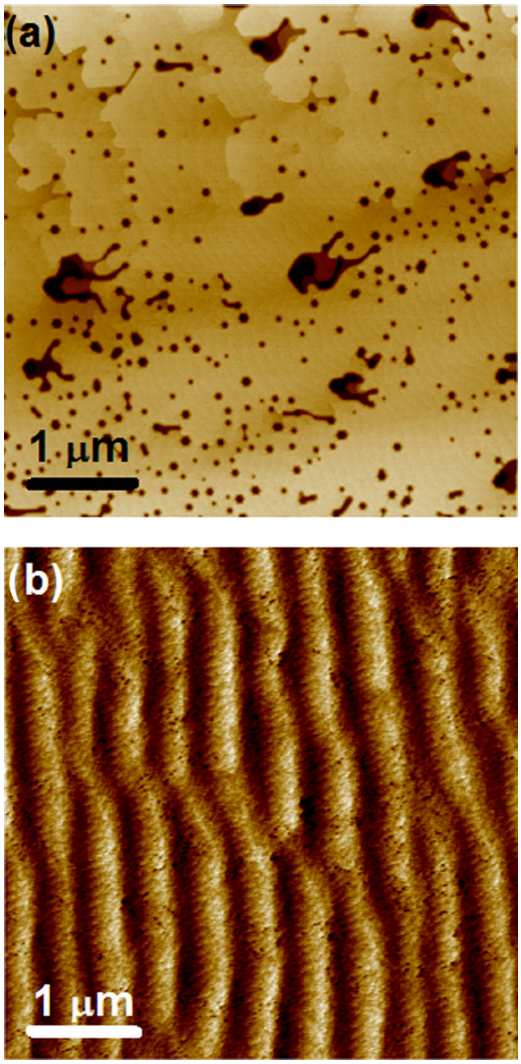

FIG. 2. (Color online) (a) AFM image of a $5 \times 5\,\mu m^2$ region of the as-grown surface near the center of the sample. The z-range is ~60 nm, and the rms roughness over this field of view is 4 nm. (b) AFM image of a $5 \times 5\,\mu m^2$ region near the center of a similarly grown sample with a lower concentration of Si in the upper contact layer. The z-range is 3 nm, and the rms roughness is 0.4 nm. The Si doping concentration of the upper contact layer is $8 \times 10^{19}\,cm^{-3}$ in (a) and $5 \times 10^{19}\,cm^{-3}$ in (b).

top 15 nm, in which it was $5 \times 10^{19}\,cm^{-3}$. The z-range and rms roughness in this image are 3 and 0.4 nm, respectively. Scattered, small pits are visible in Fig. 2(b); the depth of these pits was typically less than 1 nm. It is unlikely that the increased density in surface pits was a direct result of the higher Si doping concentration, as GaN:Si with Si concentrations as high as 1.2×10^{20} has been grown by rf-MBE without degrading the surface morphology.[14] Instead, the surface morphologies depicted in Fig. 2 appear similar to those reported by Koblmüller *et al.*,[15] in which an increasing density of surface pits on MBE-grown GaN correlated with decreasing equilibrium Ga adlayer coverage during growth. This suggests that the higher density of pits visible in Fig. 2(a) resulted from lower equilibrium Ga adlayer coverage during growth compared to the sample shown in Fig. 2(b). However, the presence of a high density of surface pits did not appear to have a deleterious effect on the electrical properties, as RTDs fabricated on the sample with the higher pit density exhibited repeatable and stable NDR, whereas those fabricated on the sample with fewer surface pits typically exhibited either inflection points in the I-V curves or weak NDR, in which the peak-to-valley current ratio (PVCR) which was only slightly greater than unity. This strongly suggests that the surface pits were confined to the upper contact layer and did not extend to the active region beneath it. Further investigation is underway to confirm this.

Cross-sectional TEM was performed on a similarly grown sample (see Fig. 3). The regrowth interface, located approximately 600 nm below the top surface, is not visible in Fig. 3(a), and no TDs were observed to have been generated either at the regrowth interface or in the AlN/GaN/AlN active region, which appears as a thin, dark, horizontal band. Figure 3(b) is a high resolution, high-angle annular dark field image of the active region. The AlN barriers are seen to be continuous and of uniform thickness. However, the mesa sidewalls exhibit a clearly visible deviation from the vertical. Vertical mesa sidewalls were obtained in later samples as a result of improvements in device processing, but the effect of the vertical sidewalls on device performance, if any, has not been determined.

Room-temperature current–voltage (I-V) measurements were performed on more than 50 RTDs across the sample. Initial bias sweeps started at −5 V on the top contact, ramped up to +6 V, and ramped down again to −5 V, all with a voltage step of 0.1 V. Various ramp rates were used but did not measurably affect device behavior. Approximately 90% of the devices tested displayed negative differential resistance, and of these, more than 90% exhibited NDR having a peak voltage within a narrow range of 4.1 ± 0.1 V. Typical peak current densities and PVCRs were $2.7\,kA/cm^2$ and 1.15, respectively. No effect of device size or lateral dimensions on the NDR was observed. Subsequent I-V measurements were carried out by sweeping the applied bias from −2.5 to +5.5 V and back to −2.5 V. Repeatable NDR was observed in the room-temperature I-V curves even after 1000 such up-and-down sweeps, as shown in Fig. 4. No indication of hysteresis, instability, or degradation of the NDR with increasing number of bias sweeps was observed.

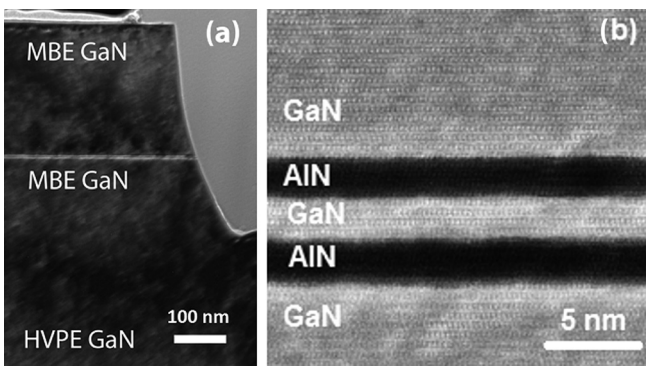

FIG. 3. Cross-sectional TEM images of a fabricated device on a similarly grown sample. Note the absence of a visible regrowth interface in (a), which is located ~600 nm below the sample surface, as well as the absence of threading dislocations generated at that interface. The 2-nm thick AlN barrier layers are clearly visible in the high angle annular dark field image (b).

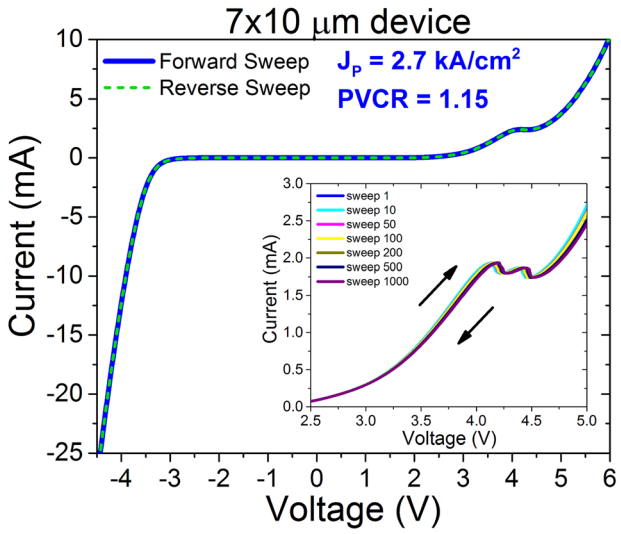

FIG. 4. (Color online) Room-temperature I-V curves of a 7 × 10 μm^2 RTD. The voltage polarity is with respect to the top contact in Fig. 1. Inset: Selected room-temperature I-V curves near the NDR region measured at the indicated number of up-and-down bias sweeps.

We speculate that several factors contributed to the improved NDR. First, improvements in device design allowed better control of injection into the quantum well states; second, improvements in processing, including sidewall passivation reduced leakage paths.[13] Finally, the use of low dislocation density native substrates allowed for the growth of homoepitaxial GaN layers and ultrathin AlN/GaN heterostructures without generating new TDs.[6,11,16] Thus, the density of TDs in the device layers is expected to be the same as that in the freestanding GaN substrates, i.e., between 10^6 and $10^7\,cm^{-2}$. Extended defects would almost certainly degrade the performance of RTDs; screw dislocations, which are thought to be conductive in GaN would provide parallel conduction pathways for leakage currents which could mask NDR and reduce the peak-to-valley current ratio, while the strain fields of both screw and edge dislocations can affect the abruptness and lateral uniformity of the interfaces between the quantum well and the barriers. On the basis of the RTDs' lateral dimensions and the TD density, one would expect to find between 0.1 and 10 TDs, on average, per device. Larger devices, which should contain a larger number of extended defects on average than smaller devices, would be expected to exhibit poorer device performance. However, no effect of device size on NDR was observed. While lower densities of extended defects are generally to be preferred, it may be that there is a threshold for TD density, below which there is no significant effect on NDR.

IV. SUMMARY AND CONCLUSIONS

We have grown an AlN/GaN/AlN RTD structure by plasma-assisted MBE on a low dislocation-density, freestanding, HVPE-grown GaN substrate. The surface of the as-grown sample was free of Ga droplets, and AFM revealed pits as well as atomic steps on the as-grown surface, suggesting low equilibrium Ga adlayer coverage during growth. These pits were likely confined to the top contact layer, as no deleterious effects on device performance were observed. TEM analysis was performed on a similarly grown sample; no new TDs were seen to have been generated from either the regrowth interface or the AlN/GaN/AlN active region. In addition, the regrowth interface was not visible, attesting to the high quality of the device layer growth.

RTDs were fabricated using optical lithography and I-V characteristics were measured on over 50 devices. Ninety percent of the devices tested exhibited NDR. Stable, repeatable, and hysteresis-free NDR was observed even after 1000 current–voltage sweeps at room temperature. This is the first report of such robust NDR in nitride RTDs at room temperature, and it indicates the promise of III-nitride based RTDs for high power, high frequency operation.

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