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Citation: Appl. Phys. Lett. **100**, 092104 (2012); doi: 10.1063/1.3684834
View online: http://dx.doi.org/10.1063/1.3684834
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v100/i9
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# High 5.2 peak-to-valley current ratio in Si/SiGe resonant interband tunnel diodes grown by chemical vapor deposition

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(Received 6 January 2012; accepted 25 January 2012; published online 28 February 2012)

Si/SiGe resonant interband tunnel diodes were fabricated using chemical vapor deposition (CVD) on 200-mm diameter p-doped silicon wafers. The resonant interband tunnel diode structure consists of a $p^+$-i-$n^+$ diode that incorporates vapor phase doped $\delta$-doping to enhance quantum mechanical tunneling probability. The tunneling barrier thickness is varied from 2 nm to 8 nm, and a record peak-to-valley current ratio of 5.2 for a CVD process is reported for a 6 nm barrier thickness with a room temperature peak tunneling current of 20 A/cm$^2$. The current density increases exponentially with spacer thickness reduction with a maximum value of 280 A/cm$^2$ for a 2 nm barrier. © *2012 American Institute of Physics*. [doi:10.1063/1.3684834]

Negative differential resistance (NDR) devices, used in conjunction with CMOS, provide a high speed, low power alternate for VLSI design.[1–3] Si/SiGe resonant interband tunnel diodes (RITD), with a CMOS compatible material system and thermal budget, provide a viable method of fabricating these devices for VLSI circuits.[4] A key requirement of NDR devices for use in embedded memory applications is a low valley current to reduce the standby power consumption while concurrently having a sufficient peak current to charge the parasitic node capacitance.[5] Hence, a large peak-to-valley current ratio (PVCR) is desired.

Quantum mechanical tunneling based NDR devices were first discovered by Esaki utilizing a degenerately doped germanium p-n junction.[6] A primary requirement for these devices is degenerately doped, abrupt doping profiles to push the Fermi level into the valence and conduction bands, respectively. RITDs accomplish this by using p and n $\delta$-doping injectors and utilized low-temperature molecular beam epitaxy (LT-MBE) in its early development to reduce dopant diffusion and segregation.[7,8] A well defined intrinsically doped Si/SiGe tunneling barrier provides the ability to tune the current density[9] with SiGe serving as a low bandgap barrier material to improve the tunneling probability. High current densities up to 218 kA/cm$^2$ (Refs. 10 and 11) and PVCR up to 6 (Ref. 12) have been achieved using LT-MBE grown devices.

Chemical vapor deposition (CVD) is the dominant epitaxial growth technique used in industrial semiconductor manufacturing allowing production of high quality single crystal films over large wafers with high growth rates and batch processing capabilities. Recently, the first CVD grown Si/SiGe resonant interband tunnel diodes were reported with a PVCR of 1.85.[13] Optimization of the boron $\delta$-doping density was performed to determine conditions to further improve PVCR to 2.95 at room temperature.[14] In this letter, the tunneling barrier thickness is varied from 2 nm to 8 nm, and the highest recorded PVCR of 5.2 is achieved at room temperature for any Si-based tunnel diode epitaxially grown by the CVD technique.

Blanket epitaxial growth of CVD-RITDs on 200 mm diameter p-Si substrates was accomplished using a standard horizontal cold wall, load-locked, ASM Epsilon™ 2000 CVD reactor with variable pressure ranging from atmospheric to reduced pressure (RP). No non-standard modifications were made to the reactor.

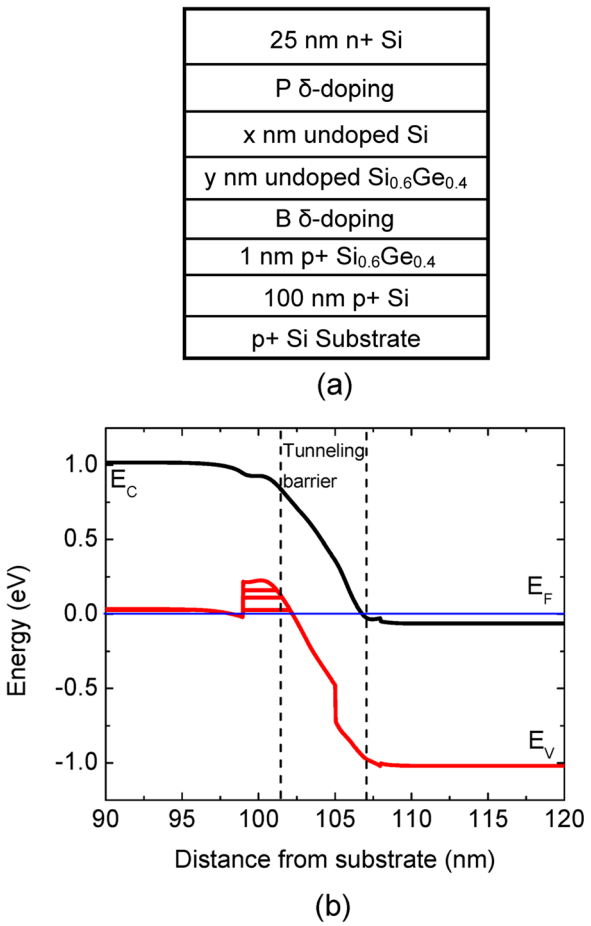


FIG. 1. (Color online) (a) Schematic diagram of the CVD-grown RITD structure with a composite Si/Si$_{0.6}$Ge$_{0.4}$ tunneling barrier. (b) Equilibrium band diagram for a 6 nm barrier device.

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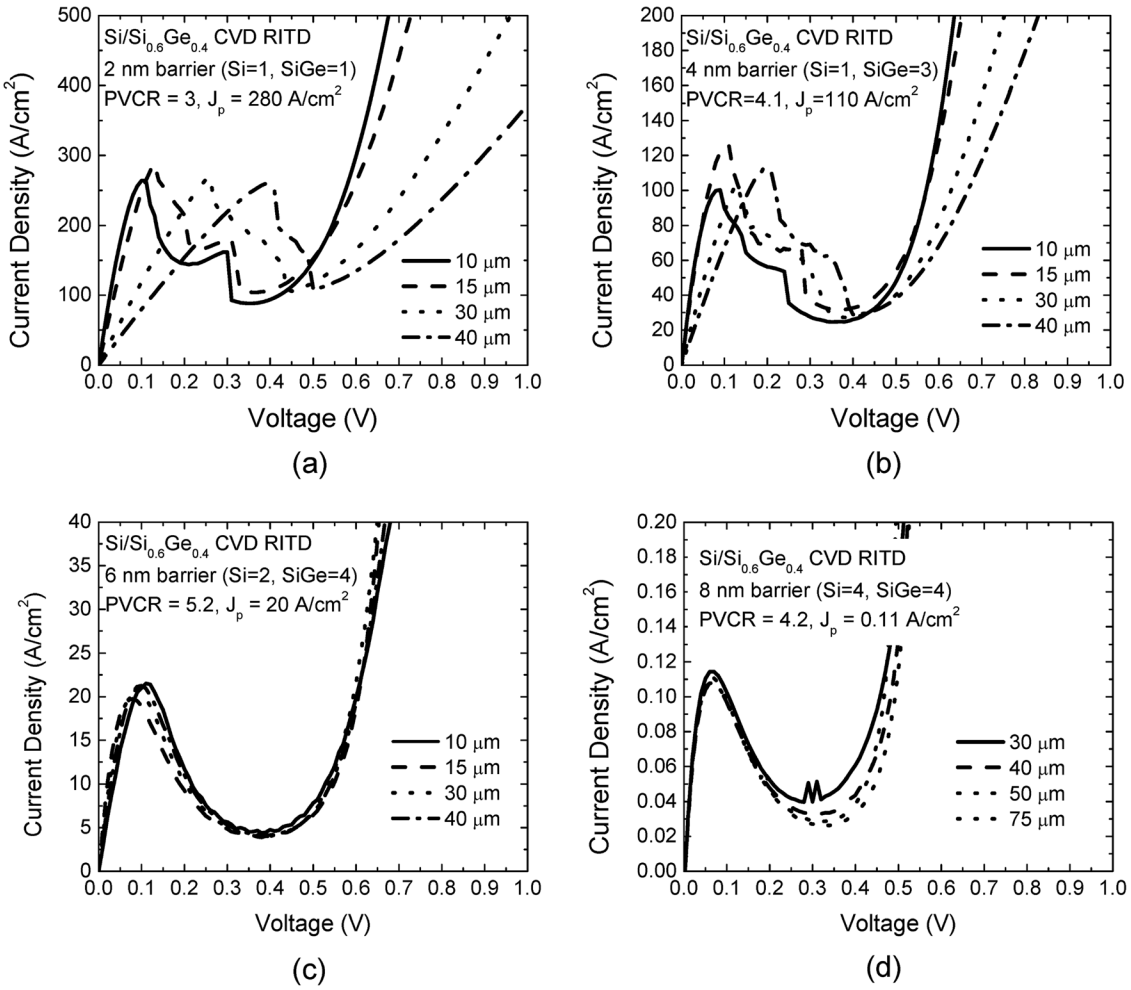


FIG. 2. Room temperature measured current-voltage characteristics for a (a) 2 nm (Si = 1 nm, SiGe = 1 nm), (b) 4 nm (Si = 1 nm, SiGe = 3 nm), (c) 6 nm (Si = 2 nm, SiGe = 4 nm), and (d) 8 nm (Si = 4 nm, SiGe = 4 nm) tunneling barrier thickness. The average peak current densities and PVCR are (a) 280 A/cm$^2$, 3; (b) 110 A/cm$^2$, 4.1; (c) 20 A/cm$^2$, 5.2; and (d) 0.11 A/cm$^2$, 4.2, respectively.

Figure 1(a) shows the nominal device structure used in this study. It consists of p and n $\delta$-doping layers creating confined quantum wells with the Si/SiGe i-layer acting as a tunneling spacer layer. Utilizing SiGe in the tunneling barrier, which has a lower bandgap, increases the tunneling probability and elevates the peak current.[8] However, its thickness is limited by the critical thickness; hence, a composite Si/SiGe tunneling spacer is employed. SiGe cladding the boron $\delta$-doping also acts as a dopant diffusion barrier suppressing interstitial diffusion of the B.[15] Concurrently, Si surrounds the phosphorus $\delta$-doping layer to suppress vacancy mediated diffusion. Growth was initiated with a 100 nm $p^+$ Si buffer layer deposited at 650 °C under RP using silane ($SiH_4$) and intentionally doped at a nominal level of $5 \times 10^{19}$ cm$^{-3}$ using diborane ($B_2H_6$). The substrate temperature was then reduced to 575 °C, and a 1 nm $Si_{0.6}Ge_{0.4}$ boron diffusion barrier layer is grown next followed by a sheet of boron (at least $5 \times 10^{13}$ cm$^{-2}$) at atmospheric pressure (AP). A nominally undoped composite $Si_{0.6}Ge_{0.4}$/Si tunneling spacer is deposited next at RP using silane ($SiH_4$) and germane ($GeH_4$). Finally, a phosphorus-spike (at least $5 \times 10^{13}$ cm$^{-2}$) is grown at 600 °C and a $n^+$ cap layer deposited at 675 °C using dichlorosilane, both at AP. The vapor phase doping technique is utilized to achieve the p and n $\delta$-doping spikes, wherein the dopant atoms are deposited on the wafer by thermal decomposition of diborane ($B_2H_6$) and phosphine ($PH_3$), respectively.[16,17] Four samples with varying spacer of $x$ nm Si and $y$ nm $Si_{0.6}Ge_{0.4}$ were grown to obtain tunneling barrier thickness of 2 nm (x = 1, y = 1), 4 nm (x = 1, y = 3), 6 nm (x = 2, y = 4), and 8 nm (x = 4, y = 4), respectively.

The device fabrication process is as follows, similar to previous reports.[14] A first photolithography step defines a series of dots with diameters of 10 $\mu$m, 15 $\mu$m, 30 $\mu$m, 40 $\mu$m, 50 $\mu$m, and 75 $\mu$m, forming the cathode contact. This is followed by electron-beam evaporation and lift-off of Ti/Au (15 nm/100nm). Mesa isolation is performed by self-aligned wet etching in a $HF/HNO_3/H_2O$ (2:100:100) solution. Finally, a second lithography step defines the anode, and Pt/Au (15 nm/100 nm) is evaporated to form the anode ohmic contact. Annealing of the contacts was deemed unnecessary and was not performed.

The calculated band diagram obtained by self-consistent solutions of Poisson and Schrödinger equations is illustrated in Fig. 1(b) and is based upon doping densities obtained from past secondary ion mass spectroscopy (SIMS) measurements of commensurate samples.[14] Quantum confinement is obtained only in the boron $\delta$-doped region with three energy

levels indicated corresponding to 2 heavy hole states and 1 light hole state. No confinement is expected in the phosphorus doping region based on prior SIMS measurements.[14] Further, the adjacent $n^+$ cap region is highly doped to reduce the series resistance but effectively leads to 3-D bulk-like degenerate doping instead on the n-side.

The measured room temperature current-voltage characteristics for each spacer thickness are shown in Fig. 2. The current density is constant for devices of different mesa area, indicating no significant surface leakage current contribution. A shift in the peak voltage with larger area for 2 and 4 nm barrier devices is due to significant contribution of series resistance as the device current increases. This is primarily due to resistance emanating from the p and n bulk regions. The peak current density scales exponentially with spacer thickness with values of 280 $A/cm^2$, 110 $A/cm^2$, 20 $A/cm^2$, and 0.11 $A/cm^2$ for thicknesses of 2, 4, 6, and 8 nm, respectively. From quantum mechanics, the tunneling probability of a particle with energy E, incident on a single potential energy barrier of height $E_0$ and width W, is given by[18]

$$T = \left[\frac{1}{1+\frac{E_0^2\sinh^2(\kappa W)}{4E(E_0-E)}}\right], \tag{1}$$

where $\kappa$ is the wave vector inside the barrier. For low tunneling probabilities, $\kappa W \gg 1$; hence, $\sinh^2(\kappa a) \sim \frac{e^{2\kappa a}}{4}$, and Eq. (1) reduces to

$$T \cong \frac{16E(E_0-E)}{E_0^2} e^{-2\kappa W}. \tag{2}$$

Tunneling probability, and hence current density, thus reduces exponentially with increasing barrier thickness. For a $p^+$-i-$n^+$ diode, this is determined by the thickness of the intrinsic region combined with the depletion width contribution of the highly doped regions. For the RITDs under study here, the tunneling distance is assumed to be the nominally undoped region sandwiched between the two $\delta$-doping spikes.

Figure 3(a) shows an exponential fit to the peak current density $J_p$ vs spacer thickness W plot obtaining a relation

$$J_P = 823 \cdot \exp(-0.54 \cdot W)\ A/cm^2. \tag{3}$$

Previous work on low-temperature MBE grown devices have demonstrated significantly higher current densities with $J_P = 2.4 \times 10^5 \cdot \exp(-0.8 \cdot W)\ A/cm^2$.[9] This can be attributed to the much sharper dopant profiles obtained from low-temperature growth and the lack of a quantum well formation in the $n^+$ region in these samples. But, by reducing the n cap doping close to the phosphorus $\delta$-doped region, a more defined 2-D quantum well can be induced which results in higher current densities at the cost of slightly increased series resistance.[19] Indeed, recent reports on $p^+$-i-$n^+$ silicon Esaki diodes grown by LT-MBE, but not utilizing $\delta$ doped p and n quantum wells, exhibit much lower current densities of 4.25 $A/cm^2$ for a 5 nm barrier thickness,[20] further declaring the benefit of a 2D-2D tunneling for maximum tunneling and utilization of SiGe as barrier material in improving the tunneling current density.

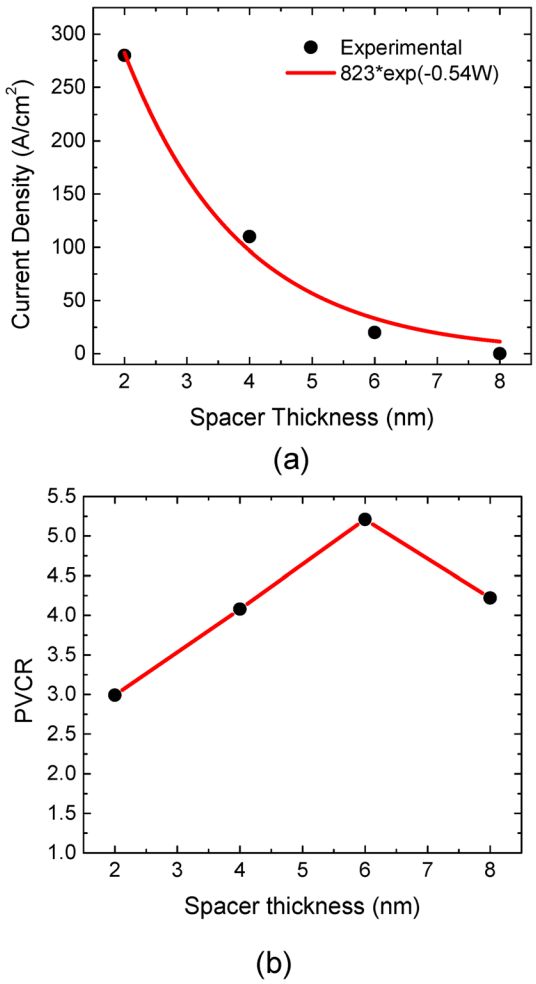


FIG. 3. (Color online) (a) Current density versus spacer thickness obtained experimentally (•) superimposed with an exponential fitting curve. (b) Maximum PVCR variation with tunneling barrier thickness.

The highest room temperature PVCR of 5.2 was obtained for the 6 nm barrier RITD and reduces for both increasing and decreasing barrier thicknesses. This is coincident with the results obtained previously on LT-MBE grown devices where a 6 nm tunneling barrier thickness yielded the maximum PVCR.[9] The valley current is primarily due to defect-assisted tunneling current also known as excess current.[21,22] Both tunneling and excess current have an exponential relation to tunneling barrier thickness. However, with an increase in tunneling distance, the excess current does not decay as rapidly as direct band-to-band tunneling current due to larger possible tunneling transitions via impurity states, and shorter tunneling distances through intermediary defect sites within the barrier. Hence, a reduction in PVCR is often observed as the spacer thickness is increased beyond 6 nm. In contrast, when the barrier is made too thin, inter-diffusion of P and B dopants into the nominally intrinsic tunneling barrier results in B-P dopant pair defect formation within the bandgap of the tunneling barrier, resulting in elevated excess currents and lower PVCR. Maximum PVCR is obtained when these two competing factors are balanced. Since CVD growth is closer to equilibrium than LT-MBE, it is expected to incorporate fewer point defects[23] and, hence, lower valley currents. This is the highest PVCR ever reported for CVD grown Si-based tunnel diodes.

In conclusion, Si/SiGe based resonant interband tunnel diodes were fabricated using CVD with varying barrier thicknesses. A record room temperature PVCR of 5.2 for CVD grown RITDs with associated peak current density of 20 A/cm$^2$ was obtained for 6 nm barrier thickness. The current density scales exponentially with barrier thickness. High PVCRs are crucial for low-power embedded memory applications to reduce standby power consumption. The ability to fabricate high PVCR devices in the Si/SiGe material system using CVD is a significant step towards achieving hybrid tunnel diode-CMOS based logic and memory circuits with large scale integration.

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