Analysis of the Voltage Swing for Logic and Memory Applications in Si/SiGe Resonant Interband Tunnel Diodes Grown by Molecular Beam Epitaxy

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***Abstract*—A method is investigated to directly engineer the voltage swing in SiGe resonant interband tunnel diodes (RITDs). Voltage swing, defined here as the voltage difference between the peak voltage and the projected peak voltage, is independent of series resistance, and thus directly impacts the noise margin in hybrid tunnel diode memory and logic applications. The three components of the total RITD current are analyzed to describe the voltage swing. The dependence of voltage swing on δ-doping concentrations and post-growth annealing temperatures in SiGe RITDs grown by low-temperature molecular beam epitaxy (LT-MBE) is investigated and the experimental results are compared with a theoretical analysis. Techniques to increase the voltage swing are discussed.**

***Index Terms*—Annealing, circuit noise, logic circuit fault tolerance, semiconductor device doping, semiconductor epitaxial layers, semiconductor junctions, tunnel diode, tunnel diode circuits.**

I. Introduction

THE TUNNEL DIODE has remarkable properties due to its folded I-V characteristics which feature both a negative differential resistance (NDR) and an ultra-high-speed transient response. These characteristics are very useful to circuit designers for applications including memory, logic and mixed signals [1]–[4]. In brief, when a tunnel diode is integrated with a transistor or two tunnel diodes are connected in series, the circuit latches to two stable operating points and switching operation or data saving can be possible between those two points. Furthermore, since the tunneling phenomenon is a majority carrier effect, the speed of circuits incorporating NDR devices can be greatly improved. Many high-performance tunnel diodes have been reported using III-V material systems [5], but the lack of an integration process compatible with complementary metal oxide semiconductor (CMOS) or SiGe heterojunction bipolar transistor (HBT) technology has limited their utility in VLSI technology. Recent work in Si-based tunnel diodes [6]–[10] and their integration with Si-based CMOS [11] and SiGe HBT [12] make these devices promising for future applications.

While peak-to-valley current ratio (PVCR) and peak current density (J_P) are common figure-of-merits used to evaluate DC performance of tunnel diodes, there is another important figure-of-merit that must be considered at the circuit level, namely, the voltage swing. It is defined as the voltage difference between the peak voltage and the projected peak voltage onto the forward biased diffusion current region [see Fig. 2(d)]. Voltage swing is an excellent indicator of the signal-to-noise margin for tunnel diode based memory and logic circuits [13], [14]. Large voltage swings make the separation between two stable operation points wider, resulting in better noise tolerance in logic and memory applications. As defined above, voltage swing, unlike voltage span which is the voltage difference between the peak and valley voltages, measures the voltage difference at the same amount of current, thus it excludes any series resistance effects which can significantly skew the voltage span. For this voltage swing study, Si-based resonant interband tunnel diodes (RITDs), which have been extensively studied by the authors [7], [8] and others [9] were used.

Si-based RITDs have tremendous flexibility to vary J_P from 20 $\mathrm{mA/cm^2}$ [15] to 218 $\mathrm{kA/cm^2}$ [8]. PVCRs typically range between 3 and 6 [7], [9] by: a) controlling the Ge composition of $\mathrm{Si}_x\mathrm{Ge}_{1-x}$ within the intrinsic barrier and each barrier layer's thickness; b) adjusting substrate growth temperature; c) adjusting post-growth annealing conditions; and d) inserting SiGe cladding layers if boron is used as the p-type δ-doping injector.

In this paper, we discuss a way to engineer the voltage swing, another figure-of-merit of NDR device that is very important in the estimation of the signal-to-noise margin for the tunnel diodes in digital circuit applications. We will show the effects of the δ-doping concentration on peak current, valley current, and the tunnel diode's voltage swing. The magnitude of the δ-doping concentrations of the injectors has been varied for this investigation and different annealing temperatures have been examined.

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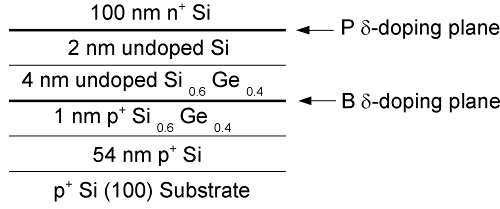

Fig. 1. Schematic diagram of the SiGe RITD structure. The key differences for each sample studied are the dopant deposition durations for both δ-doped layers, 200, 100, 50, and 25 s, which effectively equates to δ-doped sheet carrier concentrations of $1\times10^{14}\ \mathrm{cm}^{-2}$, $5\times10^{13}\ \mathrm{cm}^{-2}$, $2.5\times10^{13}\ \mathrm{cm}^{-2}$, and $1.25\times10^{13}\ \mathrm{cm}^{-2}$, respectively.

From the analysis of the peak and valley current components, a correlation between PVCR and voltage swing is also discussed.

II. Experimental

Four Si/SiGe RITDs were grown by LT-MBE and their growth conditions and device structures were designed to be identical except for both δ-doped layers described below. During the MBE growth, δ-doped layers are formed by stopping the growth (i.e., closing the Si and Ge shutters) and depositing only a dopant. The dopant concentration is usually specified by the sheet concentration and expressed in terms of $\mathrm{atoms/cm^2}$. In this paper, we also use the effective bulk dopant concentration of the δ-doped layers, expressed in $\mathrm{atoms/cm^3}$, which is determined using the assumption that the dopant atoms in the as-grown RITD are confined in a layer having a width of 1 nm. The key difference for the δ-doped layer pairs is the duration of the δ-doping deposition, 200, 100, 50, and 25 s, respectively. This variation effectively varied the δ-doped injector sheet carrier concentrations as follows: $1\times10^{14}\ \mathrm{cm}^{-2}$, $5\times10^{13}\ \mathrm{cm}^{-2}$, $2.5\times10^{13}\ \mathrm{cm}^{-2}$, and $1.25\times10^{13}\ \mathrm{cm}^{-2}$, respectively.

The epitaxial growth was carried out in a Vacuum Generators V-80 MBE system using solid sources. The basic layer structure, shown in Fig. 1, has an n-on-p growth sequence. Growths were initiated with a 2 nm undoped Si buffer layer grown at 650 °C on a Si (100) p^+ (0.015–0.04 ohm-cm) substrate (not shown in Fig. 1). The substrate temperature was lowered to 500 °C for the growth of a 54 nm B-doped p^+-Si buffer layer. After the substrate temperature was reduced to 320 °C, the remaining active device layers were grown. The growth at 320 °C includes a 1-nm B-doped SiGe, a B δ-doped layer, spacer layers consisting of 4-nm undoped SiGe and 2-nm undoped Si layers, a P δ-doped layer, and finally a 100-nm P-doped n^+-Si cap layer for ohmic contacts. During the growth, the B and P cell temperatures were kept constant at 1870 °C and 750 °C, respectively. All growth was carried out at a rate of 0.1 nm/s.

Prior to device fabrication, samples were rapid thermal annealed (RTA) at a temperature of 750 °C in a forming gas (95% $\mathrm{N_2}$/5% $\mathrm{H_2}$) ambient using a Modular Process Technology Corporation RTP-600S furnace. In order to study post-growth annealing effects, additional RTA temperatures of 700 °C, 800 °C, and 850 °C were chosen for three extra samples taken from the wafer with $1\times10^{14}\ \mathrm{cm}^{-2}$ δ-doped layers. All RTA times were fixed at 60 s. Ti/Au ohmic contacts (5, 18, 50, and 75 $\mu\mathrm{m}$ in diameter) were patterned photolithographically using liftoff and electron-beam evaporation, while backside ohmic contacts of Ti/Au were made by deposition across the full surface. Using the top contact metal as a self-aligned etch mask, all diodes were formed into a mesa structure approximately 300 nm tall. The wet etchant for mesa etching was HF:$\mathrm{H_2O}$:$\mathrm{HNO_3}$ (1:100:100) by volume ratio and etch rates varied between 100–150 nm/min.

III. Results and Discussion

A. Analysis of Key Influences on an Interband Tunnel Diode's Voltage Swing

The I-V characteristics of forward biased interband tunnel diodes consists of three current components: band-to-band tunneling current, excess current, and thermal diffusion current. In this study, on the voltage swing modulation of RITD, three different cases are considered and analyzed. All three of these cases assume that the band-to-band tunneling current component and thermal diffusion component are constant, shown in Fig. 2. However, the contribution by the excess current is varied here between the following three cases, as follows: 1) thermal diffusion current can be neglected at the projected voltage level which means the excess current dominates [Fig. 2(a) for Case I]; 2) neither thermal diffusion nor excess current can be neglected and both contribute to the projected voltage [Fig. 2(b) for Case II]; and 3) the excess current component is negligible which implies that the thermal diffusion current dominates at the projected peak voltage [in Fig. 2(c) for Case III].

As illustrated in Fig. 2, when the projected peak voltage is determined by the thermal diffusion I-V characteristics only (Case III), the largest voltage swing can be obtained, if other conditions remain unchanged. However, generally for an intrinsic Si-based RITD with zero series resistance, the projected voltage is smaller than 0.7 V [15], indicative that Case I with significant excess current often dominates. Thus, the I-V relationship of a tunnel diode for the calculation of voltage swing can be written as a combination of the peak tunneling current component and excess current component, neglecting the thermal diffusion current, because the peak voltage is primarily determined by the peak tunneling current and the projected peak voltage is primarily determined by the excess current [16]

$$\begin{aligned} I &\cong I_t + I_{ex} \\ &= I_P\left(\frac{V}{V_P}\right)\exp\left(1-\left(\frac{V}{V_P}\right)\right) + I_v\exp\left[A\left(V-V_V\right)\right] \end{aligned} \quad (1)$$

where I_t and I_{ex} are the tunneling current and excess current components, respectively. I_P and V_P are the peak current and peak voltage and I_V is the valley current at the valley voltage, V_v . A is a fitting parameter. The definition of the voltage swing, then, can be determined from the following identity:

$$\begin{aligned} &I_{V_P} - I_{V_{\mathrm{Pr}}} = I_P + I_V\exp\left[A(V_P-V_V)\right] \\ &-\left\{I_P\left(\frac{V_{\mathrm{Pr}}}{V_P}\right)\exp\left(1-\frac{V_{\mathrm{Pr}}}{V_P}\right) + I_v\exp\left[A(V_{\mathrm{Pr}}-V_V)\right]\right\} = 0. \end{aligned} \quad (2)$$

From the fact that the excess current component at $V=V_p$ and the tunnel current component at $V=V_{pr}$ (V_{pr} is projected peak voltage) are negligible, it is reasonable to now set both these

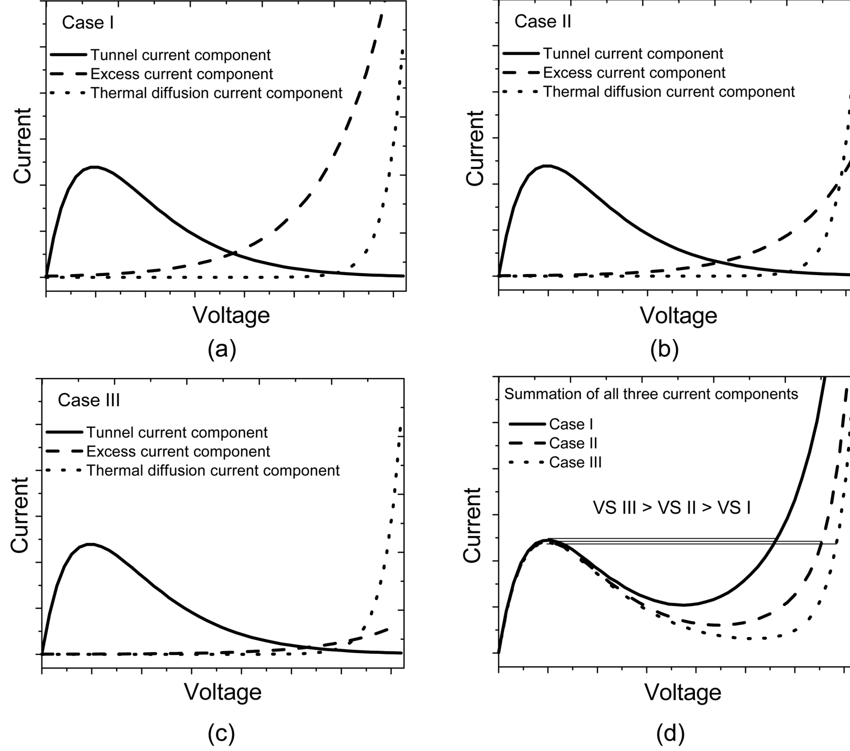

Fig. 2. The I-V characteristics of a tunnel diode consist of band-to-band tunneling, excess current, and thermal diffusion. Case I, II, and III represent different scenarios where the contribution of excess current for the tunnel diode I-V characteristics is varied relative to the thermal diffusion current. While the excess current dominates for the determination of the projected peak voltage for Case I (a), it is negligible for Case III (c) and the excess current contribution to the projected peak voltage is intermediate for (b).

terms to zero, then the voltage swing V_{SW} can be more simply expressed as

$$V_{SW} = V_{\mathrm{Pr}} - V_P \approx \frac{1}{A}\ln\frac{I_P}{I_V} + (V_V - V_P) = \left[\frac{1}{A}\ln(\mathrm{PVCR})\right] + (V_V - V_P). \quad (3)$$

The second term $V_v - V_p$ is assumed constant. This is a good approximation for the intrinsic RITD device characteristics. For instance, as the doping concentration is changed, the Fermi levels are scaled resulting in a shift of the peak and valley positions, which affect the overlap voltages. Therefore, not only will the peak voltage shift, but also the valley voltage will move by a similar scaled amount. For this approximation, no parasitic series resistance is assumed. From (3), the voltage swing is proportional to the logarithm of the I_p and I_v (or equivalently, the J_p and J_v) quotient, i.e., PVCR.

B. Role of δ-Doping Levels of an RITD on its Voltage Swing

Fig. 3 shows the δ-doping carrier concentration versus measured voltage swing, PVCR, J_P, and J_V. The sheet carrier concentration was assumed to be distributed over a 1 nm wide box for the calculations. All devices shown in Fig. 3 were post-growth annealed at 750 °C for 1 min.

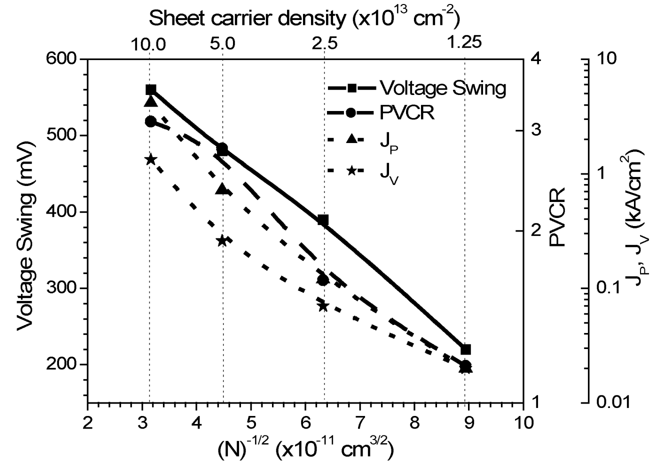

Fig. 3. Voltage swing, PVCR, J_P, and J_V versus δ-doping density showing a $N^{-1/2}$ dependence of voltage swing and $\exp(-N^{-1/2})$ dependence of J_P, J_V, and PVCR on carrier concentration, where N is an estimated bulk doping density assuming a δ-doped waist that is 1 nm in lateral extent.

The interband tunneling probability (P) [17], which determines the tunneling current, decreases exponentially with the depletion width (W)

$$I_P \propto P = \exp\left[\frac{-\left(\pi \cdot W \cdot m^{*1/2} E_g^{3/2}\right)}{\left(4\sqrt{2} q\hbar \cdot (V_{bi} - V)\right)}\right] \quad (4)$$

and W is inversely proportional to the square root of the doping concentration

$$W = \left[\frac{2\varepsilon_s}{q}\left(\frac{2}{N}\right)\cdot(V_{bi} - V)\right]^{1/2} \tag{5}$$

where $N = N_A = N_D$ in a symmetric p-n junction and ε_s is the dielectric constant of Si. The $\exp\left(-N^{-1/2}\right)$ dependence of the peak current density in these devices on the doping density was found to be in good agreement, as shown in Fig. 3, as evidenced by its slopes. It should be noted that the peak current in (4) is proportional to the maximum tunneling probability and, therefore, assumes the resonance tunneling condition is achieved regardless of the external bias necessary to bring the confined energy levels within the δ-doped regions to be coincident or the confinement energy magnitude within the quantum wells.

The excess current is given by Chynoweth [18]

$$I_{ex} \propto D_x \cdot \exp\left[\left(\frac{-\alpha_x \cdot W \cdot e^{0.5}}{2}\right)\times(E_g - eV + 0.6\cdot e\cdot(V_n - V_p)\right] \tag{6}$$

which has the same $\exp\left(-N^{-1/2}\right)$ dependence on doping density as the peak current from the depletion width, but with a different prefactor in the exponent. This dependence was observed in the relation between J_V versus doping density, as shown in Fig. 3, which implies that the excess current likely plays a significant role in many Si/SiGe RITDs. In (4)–(6), m^* is the electron effective mass, E_g is the bandgap, D_x is the density of states of defects in the forbidden bandgap, $\hbar$ is the reduced Plank constant, V_n and V_p are the Fermi energy levels on the n and p side, respectively, and α_x is a constant containing a reduced effective mass.

It can be assumed that the defect density D_x is similar amongst all the diodes plotted in Fig. 3, each having undergone identical thermal cycling during growth and annealing. Therefore, the key remaining difference amongst each of the RITDs presented in Fig. 3 rests on the doping density, embedded within the depletion width and its prefactor a in the exponent of $\exp\left(-a\cdot N^{-1/2}\right)$ in J_p and J_v, $\mathrm{PVCR} = J_p/J_v$ shows a dependence on the doping density in the same fashion as J_p and J_v, with a prefactor in the exponent that is the difference between the two. As a result, the voltage swing shows a linear dependence on $N^{-1/2}$ according to (3). This linear dependence was also observed in Fig. 3.

C. Correlation of Voltage Swing With Other Figure-of-Merits

The attribution of the excess current component to voltage swing and its correlation to the other figure-of-merits was also investigated using different annealing temperatures for the RITD with $1\times10^{14}\ \mathrm{cm}^{-2}$ δ-doping sheet carrier densities. As mentioned earlier, the main purpose of post-growth annealing is to reduce point defects created during LT-MBE growth which was adopted to suppress dopant segregation and outdiffusion from the δ-doped layers. A secondary effect of post-growth annealing on peak current component (4) arises from the effectively broadened depletion width W due to outdiffusion from the δ-doping spikes and interdiffusion and compensation within the intrinsic tunneling spacer in between [15]. This broadened depletion region causes a decrease of J_P as annealing temperature increases, shown in Fig. 4. Two parameters of excess current component in (6), the defect density of states in the forbidden bandgap, D_x, and depletion width, W are affected by post-growth annealing process.

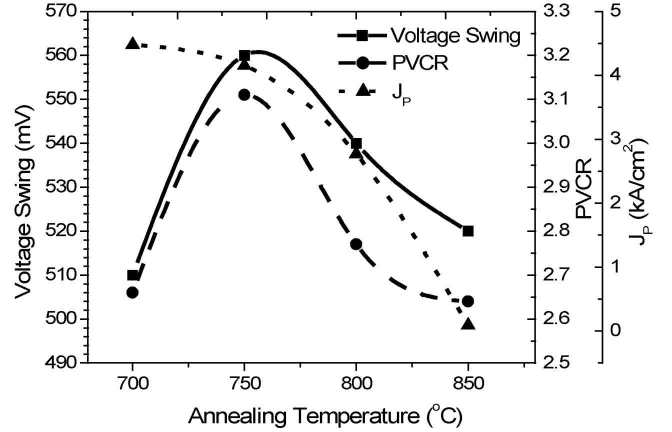

Fig. 4. Voltage swing, PVCR, I_P versus annealing temperatures. The strong correlation is observed between PVCR and voltage swing. The low PCVR despite high J_P at 700°C indicates that the defect density states in this RITD device elevates the excess current to dominate over the thermal diffusion current.

From previous studies, the defect states inside the forbidden bandgap created during LT-MBE are mostly attributed to vacancies that have distinct energy levels [19] and these defect densities were observed to be reduced by post-growth heat treatments [20]. Shown in Fig. 4 are voltage swing, PVCR, and J_P versus different post-growth RTA temperatures, 700 °C, 750 °C, 800 °C, and 850 °C. A strong correlation between PVCR and voltage swing is observed here too. It is in good agreement with a previous study on tunneling spacer thickness [15]. However, despite the highest J_P after the 700 °C anneal, the PVCR is low. This is due to the high excess current. The annealing at 700 °C was not high enough to appreciably reduce the density of vacancy defect states, D_x which, up to an anneal temperature of 750 °C, is a more important factor than the depletion-width-widening for the contribution to the excess current.

IV. Conclusion

From the study of the effects of varying δ-doping densities and varying post-growth annealing temperatures on voltage swing, the excess current I-V characteristics under forward bias dominates and determines the projected peak voltage (Case I in Fig. 2). The strong correlation of PVCR and voltage swing shown in both Figs. 3 and 4 suggests that devices with higher PVCR have smaller excess current components, therefore, their projected peak voltages are pushed closer to the regime where the thermal diffusion current is dominant, while a projected peak voltage in a lower PVCR device occurs in the range where the excess current component is dominant. Thus, it was found that the voltage swing of a tunnel diode, which determines the operational voltage range for circuit latching, should be maximized concurrently during PVCR optimization.

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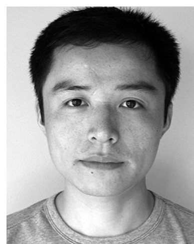

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