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Phosphorus diffusion in Si-based resonant interband tunneling diodes and tri-state logic using vertically stacked diodes

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Abstract

Various structures of Si-based resonant interband tunneling diodes (RITD) grown by low temperature molecular beam epitaxy (MBE) were studied. The results show that the peak-to-valley current ratio (PVCR) is degraded when placing SiGe layers directly adjacent to the P δ-plane. A very thin Si layer offsetting the P δ-plane and any surrounding SiGe layers is necessary.

Vertically integrated npnp Si-based RITD pairs are realized by stacking two RITDs with a connecting backwards diode between them. The *I–V* characteristics of the vertically integrated RITDs pairs demonstrate two sequential negative differential resistance (NDR) regions under forward biasing. Tri-state logic is demonstrated by using the vertically integrated RITDs as the drive and an off-chip resistor as the load.

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Keyword: Si; Resonant interband tunneling diodes; Negative differential resistance; Vertically integrated diodes; Tri-state logic

1. Introduction

As ULSI moves towards deep-submicron technology ($\leqslant$90 nm), the area, delay, and dynamic power dissipation are becoming dominated by interconnections rather than the intrinsic device speed [1]. Compared to conventional binary logic, multiple-valued logic (MVL) has a tremendous potential to overcome the limitations associated with interconnection complexity, because more information can be conveyed by multi-valued signals than binary logic, so that fewer interconnects will be required to transmit information [2]. The success of the MVL approach is greatly dependent on the availability of devices which are suitable for MVL operations. Due to the bi-state nature of conventional transistors, the resulting MVL basic building blocks are relatively complex, which would unfavorably increase device count and offset the advantages of MVL. With the unique folded *I–V* characteristics, multiple-peaked tunneling diodes are ideal for MVL implementation, because multi-level quantization and switching between several operational points can be very easily obtained.

Since MVL circuitry was demonstrated by using a multiple-peaked resonant tunneling diode (RTD) for the

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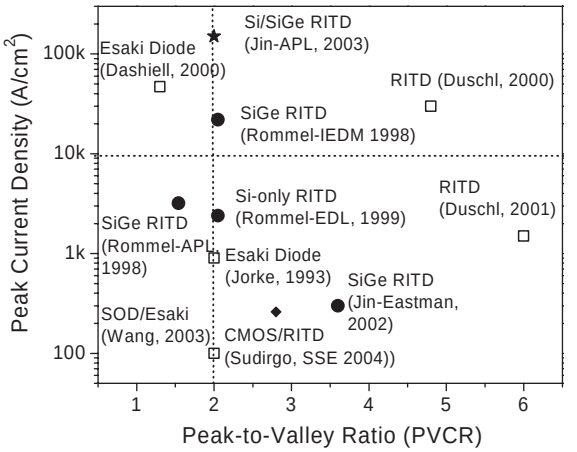

Fig. 1. A graph of PVCR plotted against the PCD of a number of Si-based interband tunnel diodes. Data points by the authors are shown as solid circles. The first CMOS integration with a Si-based interband tunnel diode by the authors is shown as a diamond. Data points from other research groups are shown as open squares.

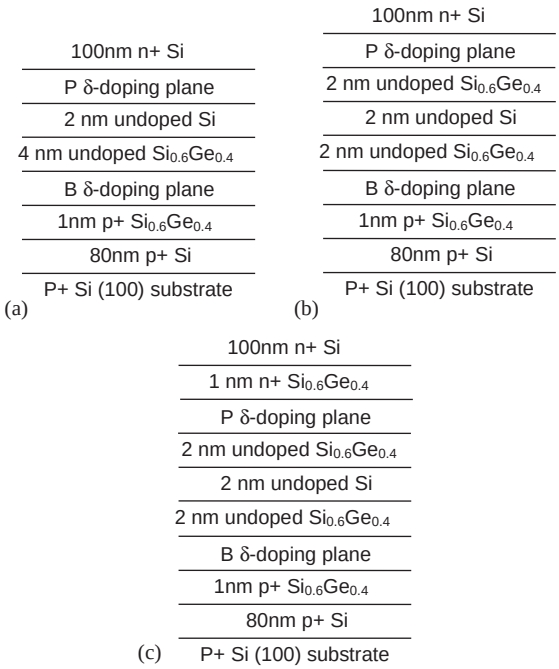

Fig. 2. Structures of the Si-based RITDs used in this study. (a) structure A; (b) structure B; (c) structure C.

first time [3], many RTD-MVL circuits, such as multi-valued memory cell, analog-to-digital converters (ADC), counter, decoder, and programmable logic array (PLA) ([4,5] and references therein) with greatly reduced complexity and component count have been reported. Ultra-high circuit speed is also achievable due to the picosecond switching speed of multiple-peaked RTDs. However, all these above-mentioned multiple-peaked RTDs utilize III–V semiconductors, which are not compatible with mainstream Si technology. The recent development of Si-based resonant interband tunneling diodes (RITD) [6–8] and successes in monolithic integration of RITDs [8–11] show great potential for their integration with CMOS transistors [8,11] and Si/SiGe heterojunction bipolar transistor (HBT) technology [9] for highly functional tunnel diode-transistor circuits. Fig. 1 summarizes these results by plotting the PVCR against its corresponding peak current density (J_p) for a number of previously reported Si-based interband tunnel diodes [6–8,10–18]. In this paper, our present work aiming at higher PVCRs and the first double peaked Si-based tunneling structure, in a vertical stack which is suitable for MVL operations. A tri-state logic circuit was then demonstrated using the RITD pair and an external resistor.

2. Experimental

The structure of a typical Si-based RITD is shown in Fig. 2(a) [8]. The spacer layer sandwiched between the two δ-doping layers is comprised of two layers, an intrinsic Si layer of 2 nm thick which is below the P δ-doping layer and an intrinsic $Si_{0.6}Ge_{0.4}$ layer of thickness 4 nm that is above the B δ-doping layer. Note, there are thin $Si_{0.6}Ge_{0.4}$ cladding layers surrounding the B δ-doping layer in order to suppress the B outdiffusion, so that the sharp B peak can be maintained during the growth and short 1-min post-growth annealing. As a result, the Si/SiGe RITDs have an elevated thermal budget to more effectively remove point defects within the spacer [19], so that the valley current will be decreased, which leads to a higher PVCR [8].

The entire vertically integrated RITD pair was grown by low-temperature molecular beam epitaxy (MBE) using elemental Si and Ge in electron-beam sources on 75 mm B-doped ($\rho = 0.015$–$0.04\,\Omega$ cm) Si (1 0 0) wafers. The doping levels for both n^+ and p^+ layers are $5 \times 10^{19}\,cm^{-3}$, while both the B and P δ-doping sheet concentrations were maintained at $1 \times 10^{14}\,cm^{-2}$. Prior to device fabrication, portions of the grown wafers were rapid thermal annealed (RTA) using a forming gas ambient (N_2/H_2) in a Modular Process Technology corporation RTP-600S furnace at various temperatures for 1 min. Ti/Au dots with various diameters were patterned on the surface of the wafers via standard contact lithography and liftoff. A buffered oxide etch was used prior to metallization. Using the metal dots as a self-aligned mask, HF/HNO_3 wet etching was performed to isolate the diodes into mesas. Finally, a Ti/Au backside contact was evaporated on all of the samples.

3. Results and discussions

3.1. The effect of SiGe layers cladding P δ-doping layer

Given the fact that an improved PVCR can be obtained by cladding B δ-doping layer with SiGe layers [8], it is then of interest to attempt cladding of the P δ-doping layer to suppress P out-diffusion. Three structures were designed to study the effect of Si and SiGe cladding layers around the P δ-doping layer. All structures maintained the intrinsic layer thickness of 6 nm, which to first order determines the tunneling distance. Fig. 2(a) shows Structure A, the control sample with Si only cladding, which has active layers of 1 nm $Si_{0.6}Ge_{0.4}$/B δ-plane/4 nm $Si_{0.6}Ge_{0.4}$/2 nm Si/P δ-plane. Fig. 2(b) shows Structure B with Si and SiGe cladding, which has active layers of 1 nm $Si_{0.6}Ge_{0.4}$/B δ-plane/2 nm $Si_{0.6}Ge_{0.4}$/2 nm Si/2 nm $Si_{0.6}Ge_{0.4}$/P δ-plane. Compared to Structure A, the 4 nm $Si_{0.6}Ge_{0.4}$ layer was split into two 2 nm $Si_{0.6}Ge_{0.4}$ layers, and the P δ-plane is directly grown atop of the $Si_{0.6}Ge_{0.4}$ layers without the thin Si offset layer. Fig. 2(c) shows Structure C with SiGe only cladding, which has active layers of 1 nm $Si_{0.6}Ge_{0.4}$/B δ-plane/2 nm $Si_{0.6}Ge_{0.4}$/2 nm Si/2 nm $Si_{0.6}Ge_{0.4}$/P δ-plane/1 nm $Si_{0.6}Ge_{0.4}$. Compared to Structure B, there is an additional 1 nm $Si_{0.6}Ge_{0.4}$ grown atop of the P δ-plane, so that the P δ-plane is effectively clad entirely by $Si_{0.6}Ge_{0.4}$ layers.

Fig. 3 shows the PVCR vs annealing temperature for each structure. Structure A exhibited the highest PVCR of 3.05 using 1-min annealing at 800 °C, which is substantially higher than the performance of Structure B (PVCR of 2.02 by 800 °C annealing), which has a $Si_{0.6}Ge_{0.4}$ layer directly adjacent to one side of P δ-plane. Structure C, in which both sides of P δ-plane are clad by $Si_{0.6}Ge_{0.4}$ layers, shows a PVCR of only 1.90 using 750 °C annealing, which is more degraded than Structure B. The data clearly shows that PVCR is substantially degraded when placing SiGe layers directly adjacent to the P δ-plane.

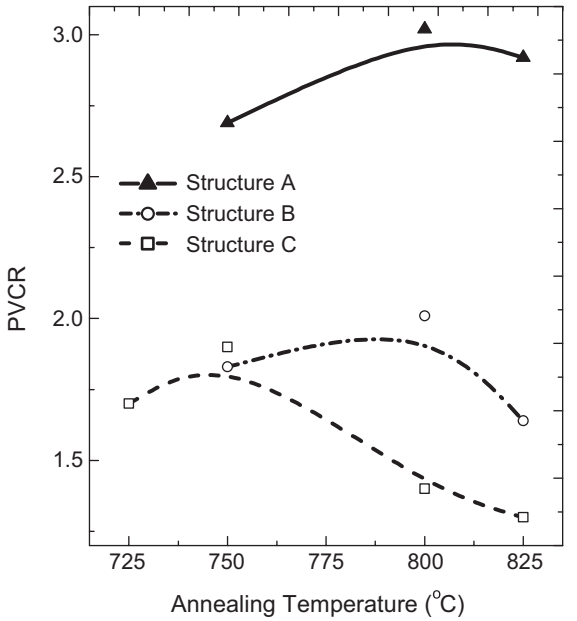

Fig. 3. PVCR as a function of annealing temperature for each structure.

The degradation caused by the proximity of SiGe layers can be explained as follows: First, P diffusion is slightly enhanced by SiGe layers cladding the P delta doping layer, which is confirmed by a recent study of P diffusion in compressively strained SiGe layers [20]. The increased P diffusivity in compressively strained SiGe layers results from both chemical effect and strain effect. As a result, the δ-doped quantum well formed by the P δ-plane will lose its confinement faster in Structure B and C than Structure A. Furthermore, the faster diffusion of the P atoms will lead to more P–B dopant pairs formed within the nominally intrinsic tunneling barrier, which provides energy levels within the forbidden energy bandgap for electrons to tunnel through as part of the excess current component [21]. Consequently, as the undesired excess current component rises, the PVCR is reduced. Secondly, the compressive strain in the SiGe layers which clads the P δ-plane will result in a band offset [22] that unfavorably reduces, rather than increases, the quantum well height formed by P δ-plane. In conclusion, a thin Si layer offsetting the P δ-plane and SiGe layer is necessary to obtain high PVCR.

3.2. Vertically integrated RITD pairs and demonstration of tri-state logic

Fig. 4(a) shows the building block for the vertically integrated RITD pairs. Note, there is a 4 nm Si offsetting layer between the $Si_{0.6}Ge_{0.4}$ layer and the P δ-plane. Fig. 4(b) shows the structure of the vertically stacked RITDs with an npnp configuration. The top RITD and bottom RITD have the same spacer

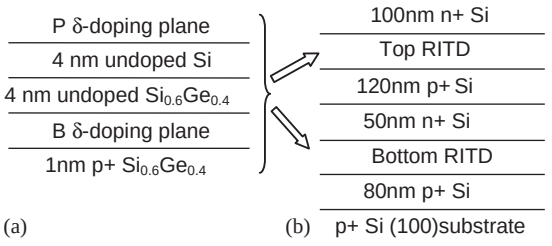

Fig. 4. (a) Schematic of the Si-based RITD as a building block, and (b) schematic of the vertically stacked RITD pair using an npnp configuration of two generic Si-based RITDs connected serially by a backwards diode.

configuration in order to obtain similar PVCR and J_p values. Note, there is a backward diode between the top diode and bottom diode, which will be reverse biased and should effectively connect the top RITD and bottom RITD with a small series resistance under the forward biasing condition for the vertically stacked RITDs.

Fig. 5 shows the *I–V* characteristics of the vertically integrated RITD pair after a 825 °C, 1 min anneal. Double NDR regions in the forward biasing condition were observed, with one diode showing a PVCR of 3.25 and J_p of 0.37 kA/cm^2, and another diode showing a PVCR of 3.21 with J_p of 0.39 kA/cm^2. Note, the peak voltage of the first NDR region occurs around 1.2 V, which is much higher than the 0.1–0.2 V observed for discrete RITDs, shown in Fig. 2(a) [6–8]. A large series resistance is causing the shift which the authors attribute to the reverse biased backwards diode. This resistance leads to a hysteresis when sweeping the voltage in forwards and backwards directions, which was also observed in previous RTD reports [23]. Improvements to the design of the backwards diode leading to a reduction of this series resistance should be possible with further optimization.

To demonstrate tri-state logic, the vertically stacked RITD pair was combined with a resistor. The stacked RITD pair operated as the drive and a 1 kΩ off-chip resistor as the load, as shown schematically in Fig. 6(a). The load line analysis of the circuit with a representative stacked RITD pair and 1 kΩ resistor is shown in Fig. 6(b). The initial operating point of the tri-state latch is P1 by biasing V_{pulse} with a DC bias of 5.8 V, a positive

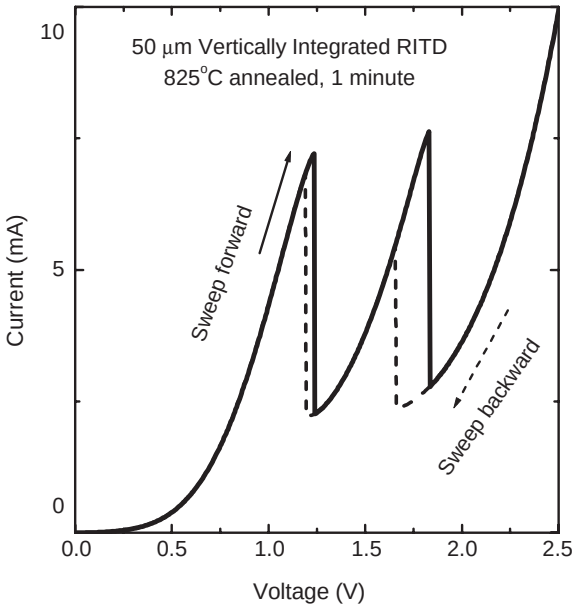

Fig. 5. *I–V* characteristics of the vertically stacked RITD pair.

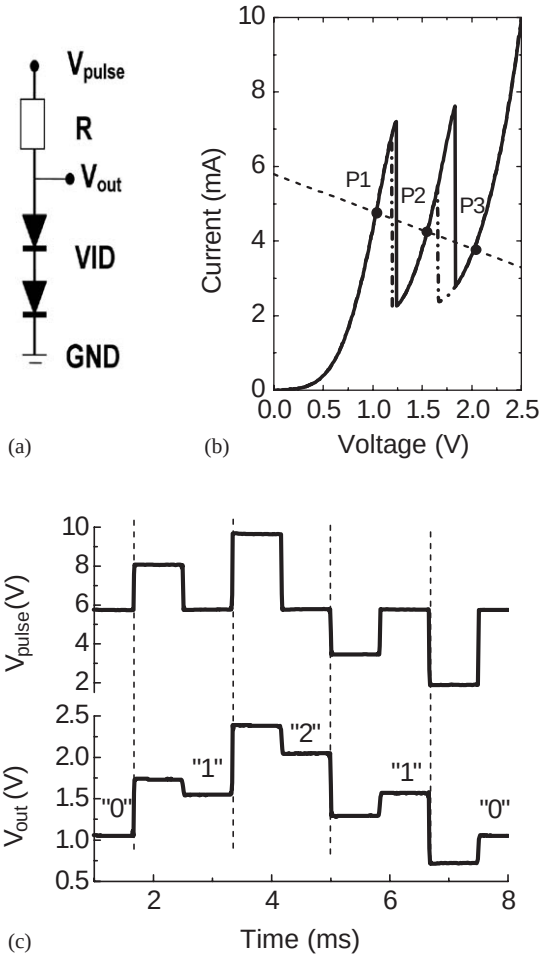

Fig. 6. (a) Circuit schematics; (b) load line analysis of the circuit with a representative vertically stacked RITD pair as the drive and 1 kΩ resistor as the load; (c) oscilloscope capture of the resulting waveform with V_{pulse} and V_{out} showing tri-state logic functionality.

triggering pulse is then fed to the resistor to momentarily lift the load line past the first peak and the operating point is moved to P2 at the trailing edge of the pulse. Note, that during this "write" operation, V_{out} deviates slightly from P2, until V_{pulse} is returned to its quiescent state of 5.8 V. An even higher triggering pulse then allows P3 to be accessed. Similarly, negative pulses based on the DC bias of 5.8 V can lower the load line pass the valley region and shift the operating point backwards, stepping down from P3 to P2 or P1. Fig. 6(c) shows the resulting waveform of the state transitions from "0" to "1", "1" to "2", "2" to "1" and "1" to "0", effectively demonstrating the tri-state latching operation. The "0", "1" and "2" latched states correspond to 1.05, 1.55 and 2.04 V, respectively. Note, the intermediary point P2 can be bypassed when moving between

states P1 and P3, although this operation is not shown here. Intrinsic switching speeds were not evaluated at this time as the circuit should be limited by the parasitics associated with the external resistor. A monolithic transistor would be the preferred load and provide for faster switching operation. With the recent development of Si-based RITD exhibiting peak current density as high as 151 kA/cm^2 [12], over 10 GHz switching speed for a 3 V voltage swing is possible.

4. Conclusion

PVCR is degraded by growing SiGe layers directly adjacent to the P δ-plane, and a thin Si layer offsetting the P δ-plane from the surrounding SiGe layers is necessary. A vertically integrated Si-based resonant interband tunneling diode (RITD) pair was successfully built with PVCRs above 3.2. Double NDR regions in the forward biasing condition were observed. Tri-state logic was demonstrated by a breadboarded circuit using the vertically integrated RITD pair as the drive and an off-chip resistor as the load.

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