Improved vertically stacked Si/SiGe resonant interband tunnel diode pair with small peak voltage shift and unequal peak currents

N. Jin, S.Y. Chung, R. Yu, P.R. Berger and P.E. Thompson

A vertically integrated and serially connected *npnp* Si-based resonant interband tunnelling diode (RITD) pair is realised with low temperature molecular beam epitaxy (MBE) by monolithically stacking two RITDs with different spacer thicknesses. The asymmetric design manifests as unequal peak current densities that provide for much larger and uniform separation of the holding states for multi-valued logic. A δ-doped backwards diode connects the two serially connected RITDs with a very small series resistance. The *I–V* characteristic of the improved vertically integrated RITDs demonstrates two negative differential resistance (NDR) regions in the forward biasing condition with a small peak shift and unequal peak currents.

Introduction: As ULSI moves towards deep-submicron technology ($\leq$90 nm), interconnections rather than intrinsic device characteristics dominate the area, delay, and dynamic power dissipation [1]. Compared to conventional binary logic, multiple-valued logic (MVL) has a tremendous potential to overcome the limitations associated with interconnection complexity [2].

Many MVL circuits, such as multi-valued memory cell, analogue-to-digital converters (ADCs), counter, decoder and programmable logic array (PLA) [3, 4 and references therein] with greatly reduced complexity and component count have been demonstrated using III–V resonant tunnelling diodes (RTDs). Ultra-high circuit speed is also achievable owing to the picosecond switching speed of multiple-peaked RTDs. The first double peaked tunnelling structure in an Si platform was recently demonstrated [5] by vertically integrating two serially connected Si-based resonant interband tunnelling diodes (RITD) [6–8] with a connecting backward diode. A simple tri-state logic circuit was then demonstrated using the RITD stack and an external resistor [5]. However, two issues associated with that vertically integrated Si-based RITD design will be addressed here: (i) Since the two RITDs exhibit almost identical peak currents and valley currents, the pair is more susceptible to noise interference when using a constant-current-source as the load. For example, to make the transition from state '0' to '1', the pulse lifting up the flat load line to pass the first peak may accidentally pass the second peak and reach state '2' with the presence of noise; (ii) A large nonlinear series resistance originated from the backward diode that is needed to serially connect these two bipolar devices without concurrently introducing a reverse biased rectifying junction in series. A significant shift in the peak voltage positions to higher values resulted, which would lead to a larger power consumption. To solve these problems, a modified vertically integrated RITD pair with unequal spacer thicknesses and a δ-doped backward diode was realised. In this Letter, we report on the improved Si-based vertically integrated and serially connected RITD pair showing small peak shifts and unequal peak currents.

Experiment: Fig. 1*a* shows the generic structure of the vertically stacked RITDs with an *npnp* configuration. The backward diode connecting the top diode and bottom diodes will be reverse biased and effectively connects the top diode and bottom diode as a small series resistance under forward bias for the vertically stacked RITD pair. The generic structure of the Si-based RITD [8] is shown in Fig. 1*b*. The doping level for both n^+ and p^+ layers are 5×10^{19} cm^{-3}, while both the B and P δ-doping sheet concentration was maintained at 1×10^{14} cm^{-2}.

In the previous study [5], the top RITD and the bottom RITD share the same spacer configuration with L_1 of 4 nm and L_2 of 4 nm, which leads to nearly identical peak currents and valley currents of these two diodes. In this study, the spacer configuration of the upper RITD was slightly modified with L_1 increased from 4 to 4.2 nm, while the lower RITD was unchanged. The purpose of this modification is to lower the peak and valley current of the upper RITD to facilitate a transistor-type load, while keeping the peak current of the upper RITD greater than the valley current of the lower RITD to ensure tri-state logic operation.

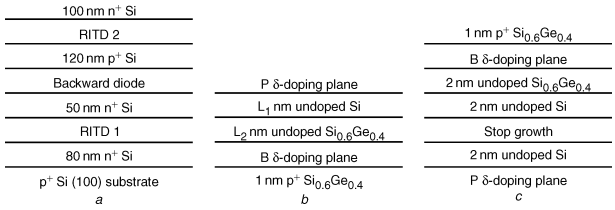

Fig. 1 *Schematics*

a Schematic of Si-based vertically stacked and serially connected RITD pair using *npnp* configuration in this study
b Schematic of generic structure of Si-based RITD
c Schematic of δ-doped backward diode structure

The backward diode in the previous study was formed between the p^+ injector layer of the top RITD and the n^+ injector layer of the bottom RITD, which is essentially a *pn* junction with doping levels on both sides of 5×10^{19} cm^{-3} and no intrinsic spacer between the *p* and *n* sides. The relatively low doping density of both sides plus dopant diffusion during the 825°C 1-minute post-growth rapid thermal annealing resulted in a wide tunnelling barrier and a large nonlinear resistance, which unfavourably shifted the first peak to around 1.2 V.

In this study, a δ-doped backward diode is used to obtain a significantly higher doping density and a thinner tunnelling barrier, as shown in Fig. 1*c*. Both the B and P δ-doping layers have a sheet concentration of 0.25×10^{14} cm^{-2}. A 6 nm intrinsic Si/SiGe spacer is inserted between the δ-doping layers to prevent dopant interdiffusion and compensation. However, it can be problematic to grow B-doped layers on top of a P δ-doping layer owing to P segregation if no precautions are taken. Segregated P atoms can incorporate into the overlayer and lead to an unintentionally doped spacer and compensate the B-doped layer which will result in a smaller effective doping density. To minimise the effect of P segregation on both the backward diode and the upper RITD, a stop growth technique associated with a substrate temperature reduction to 320°C to control the P segregation [9] was employed.

The entire vertically integrated RITD pair was grown by low temperature MBE using elemental Si and Ge in electron-beam sources on 75 mm B-doped ($\rho = 0.015$–$0.04\ \Omega \cdot$ cm) Si (100) wafers. Prior to device fabrication, portions of the grown wafers were rapid thermal annealed (RTA) using a forming gas ambient (N_2/H_2) in a Modular Process Technology Corporation RTP-600 S furnace at various temperatures for 1 min. Details of the fabrication process can be found in [5, 6, 8].

Results: Fig. 2 shows the *I–V* characteristics of the modified RITD pair with an 18 μm mesa diameter and post-growth annealed at 835°C for 1 min. The large first and second peak voltages, 1.225 and 1.825 V, respectively, previously observed in the *I–V* characteristics [5] are now greatly reduced, with the first peak occurring at 0.235 V and the second peak occurring at 0.975 V. No hysteresis was observed in the NDR region. Etching was performed to isolate each *pn* junction and characterise them separately. The zero bias junction resistance of the backward diode is determined to be 71 k$\Omega \cdot \mu$m^2, which is about 350 times less than the zero bias junction resistance of the backward diode in the previous study, 25 M$\Omega \cdot \mu$m^2 [5]. The zero bias junction resistances of the upper and lower RITDs are 56 and 20 k$\Omega \cdot \mu$m^2, respectively, which are comparable to the backward diode. Therefore, the peak voltage shift is greatly reduced in this study. *I–V* characteristics of the upper diode shows a PVCR of 3.5 with J_p of 155 A/cm^2, and the lower diode shows a PVCR of 3.6 with J_p of 515 A/cm^2. The slightly suppressed PVCR of the upper RITD may be due to some residual segregation of P from the backward diode despite the reduced growth temperature of 320°C during the top layers or the prolonged reduced substrate temperatures. The unequal spacer thickness of the two RITDs results in differences in the peak and valley current differences between the upper and lower RITDs, compared with the original vertically integrated RITD pair [5]. The peak current difference is 0.68 mA and the valley current difference is 0.18 mA. This feature makes the modified RITD pair more suitable for circuit implementation using a constant-current-source load, such as a transistor. A current source load of 0.5 mA would result in three stable operational points, which are 0.17, 0.76 and 1.29 V, respectively.

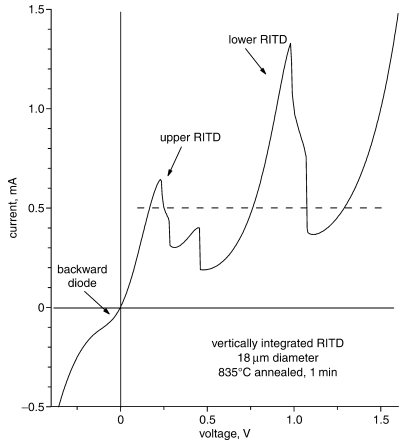

Fig. 2 *Measured I–V characteristics of vertically stacked RITD pair*
- - - - load line of 50 mA current source

Conclusion: A vertically integrated and serially connected *npnp* Si-based RITD pair was successfully built with PVCRs above 3.5. Double NDR regions under forward bias were observed. Small shifts in the peak voltage were obtained to lower power consumption by modifying the backward diode. Unequal peak currents facilitate circuit implementation with constant-current-source loads.

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