# 151 kA/cm$^2$ peak current densities in Si/SiGe resonant interband tunneling diodes for high-power mixed-signal applications

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Room-temperature $I$–$V$ characteristics of epitaxially grown Si/SiGe resonant interband tunneling diodes (RITDs) with extremely high peak current densities are presented. By optimizing the physical design, doping concentrations, and post-growth anneal temperatures, RITDs having peak current densities over 150 kA/cm$^2$, peak-to-valley current ratios (PVCRs) greater than 2, and an estimated speed index of 34 mV/ps have been obtained. The interplay among the conditions to achieve maximum current density and highest PVCR is discussed. This result demonstrates the high potential of this type of Si-based tunnel diode for high-power mixed-signal applications. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1618927]

The union of tunnel diodes with transistors can increase circuit speed, reduce component count, and lower power consumption due to the unique property of the tunnel diode's negative differential resistance (NDR), which leads to novel quantum nonlinear functional devices and circuits.[1–3] The end result is more computational power per unit area than a transistor-only circuit topology by harnessing the tunnel diode's folded $I$–$V$ characteristics. These types of hybrid circuits have already been demonstrated in many III-V compound semiconductor material systems in which significant conduction band (CB) offsets facilitate double-barrier resonant tunneling diodes (DBRTDs) using intraband tunneling within the CB.[4] Some useful mixed-signal circuit applications using III-V DBRTD transistor/tunnel diode topology that require high current density tunnel diodes are compact A/D converters[2] and oscillators for wireless applications.[3] Tunnel diodes would also be an attractive addition to Si-based transistors, such as complementary-metal-oxide-semiconductor (CMOS) and Si/SiGe heterojunction-bipolar transistors (HBTs) if a viable Si-based tunnel diode could be added to the CMOS/HBT process flow using a simple and benign process.[1] This could have enormous impact on future Si technology beyond the 90-nm node, especially a high current density Si-based tunnel diode that could boost Si-based wireless technology.

Until recently, a Si-based tunnel diode suitable for monolithic integration with ultralarge-scale integration has eluded realization. However, recent developments in Si-based tunnel diode technology by the authors[5–8] and other researchers[9–12] are challenging this roadblock by switching to an interband tunnel diode configuration that requires degenerate doping instead of CB offsets. Further, the valley current of interband tunnel diodes is governed by inelastic scattering only, while the valley current of intraband tunnel diodes is determined by both elastic and inelastic scattering.[13] Using conventional epitaxial growth conditions, it is difficult to achieve such a high level of doping. This was overcome by use of low-temperature molecular-beam epitaxy (LT-MBE), which suppressed dopant segregation effects to realize a Si-based resonant interband tunnel diode (RITD) that is actually a hybrid of features from both an RTD and an Esaki diode.[5]

In this letter, we report on work to maximize the peak current density ($J_p$) of Si-based RITDs to achieve a target value of $\geq 50$ kA/cm$^2$, concurrently with a reasonable peak-to-valley current ratio (PVCR) for future mixed-signal applications. Specifically, this letter will present current density results for Si-based RITDs that exceed 150 kA/cm$^2$, concurrently with a room-temperature PVCR over 2. This reported peak current density is substantially higher than the previously reported results for Si-based interband tunnel diodes.[5–14] This result was achieved by a careful engineering of the tunnel diode spacer thickness and the process temperatures.

The basic structure, shown in Fig. 1, of the Si-based RITDs was grown by LT-MBE.[8] The spacer layer sandwiched between the two $\delta$-doping layers is comprised of two layers: an intrinsic Si layer of thickness $L_1$ which is below the P $\delta$-doping layer, and an intrinsic Si$_{0.6}$Ge$_{0.4}$ layer of thickness $L_2$ that is above the B $\delta$-doping layer. The RITDs studied here varied the overall spacer thicknesses over 6 nm ($L_1 = 2$ nm/$L_2 = 4$ nm), 5 nm ($L_1 = 1.5$ nm/$L_2 = 3.5$ nm), 4 nm ($L_1 = 1$ nm/$L_2 = 3$ nm), 3 nm ($L_1 = 1$ nm/$L_2 = 2$ nm), 2 nm ($L_1 = 1$ nm/$L_2 = 1$ nm), and 1 nm ($L_1 = 0.5$ nm/$L_2$

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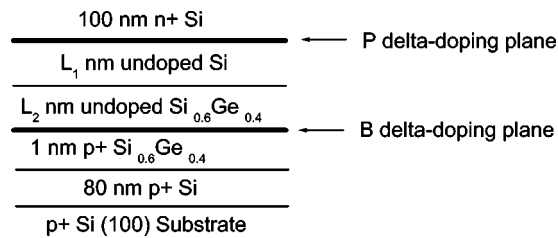
FIG. 1. A schematic of the basic RITD structure used in this study.



FIG. 3. Band diagram of Si/SiGe RITD at an applied bias of 0.4 V showing CB longitudinal ($X_z$) and transverse ($X_{xy}$) valleys and HH, LH, and split-off-hole bands.

$=0.5$ nm). Note there are SiGe cladding layers surrounding the B $\delta$-doping layer in order to suppress the B outdiffusion, so that the sharp B peak can be maintained during the growth and short 1-min post-growth annealing. As a result, the Si/SiGe RITDs have an elevated thermal budget to remove the point defects within the spacer more effectively, so that the valley current will be decreased, which leads to a higher PVCR.[8] In addition, the inclusion of a SiGe alloy to the tunnel spacer acts to increase momentum mixing, which enhances tunneling probability and current density provided the critical thickness is not exceeded.

Epitaxial growth was achieved with an MBE growth system using elemental Si and Ge in electron-beam sources. The structures were grown on 75-mm B-doped ($\rho = 0.015 - 0.04~\Omega$ cm) Si (100) wafers. The doping level for both $n^+$ and $p^+$ layers is $5 \times 10^{19}$ cm$^{-3}$, while the B $\delta$-doping sheet concentration was maintained at $1 \times 10^{14}$ cm$^{-2}$ and the P $\delta$-doping sheet concentration was varied from $1 \times 10^{14}$ to $3.4 \times 10^{14}$ cm$^{-2}$. For detail fabrication process, refer to Refs. 5–8.

An array of RITD samples with varying spacer thicknesses, keeping the P $\delta$-doping sheet concentration at $1 \times 10^{14}$ cm$^{-2}$, were annealed at 600, 700, and 775 °C for 1 min. It is observed that there is a tradeoff between high $J_p$ and high PVCR, shown in Fig. 2. From the data, it is evident that at each spacer thickness there is an optimal annealing temperature for maximum PVCR and a set of lower annealing temperatures for more elevated peak current densities. A maximum PVCR is reached by annealing the sample at the highest annealing temperature possible, to effectively remove the point defects created by the LT-MBE process that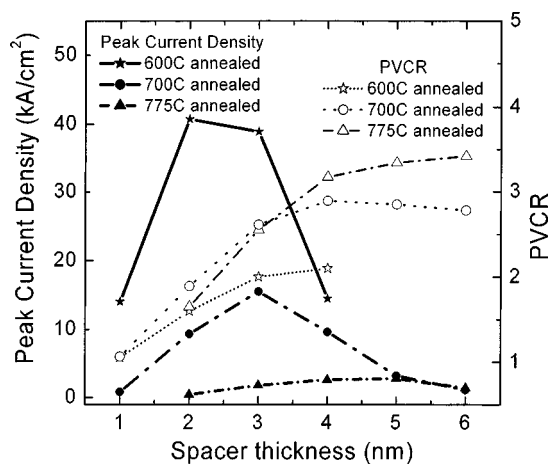 contribute to a defect-related tunneling valley current component, before diffusion of the $\delta$-doping layers and Ge within the tunneling spacer results in a marked modification to the original structure.

For instance, the sample with a 2-nm spacer has its maximum peak current density of 42 kA/cm$^2$ and PVCR of 1.6 when annealed at 600 °C for 1 min. The rolloff of $J_p$ as the spacer thickness is reduced below 3 nm, shown in Fig. 2, is indicative of the interdiffusion at the $p-n$ junction that results in an actual increase in the depletion width, and subsequently the tunneling distance and therefore a reduction in tunneling probability. We modeled this using standard diffusion theory. The optimal spacer thickness for high peak current density decreases if the annealing temperature is lowered and interdiffusion is suppressed. Generally, below a nominal spacer thickness of 4–6 nm, the PVCR decreases as the spacer becomes thinner, as shown in Fig. 2, which indicates that the reduction in the spacer thickness acts to reduce the desired tunneling selection rules and to enhance the probability of tunneling through defect sites.

The offsetting trends of PVCR and $J_p$ versus spacer thickness indicate the tradeoff between high PVCR and high $J_p$. It is desirable that RITDs with high $J_p$ should also show reasonable PVCR. Since $(J_p - J_v)$ figures so prominently in both the maximum rf power and the speed index, this factor, which represents the available current density swing, should be optimized.

Considering the device performance of the RITD, both PVCR and $J_p$ are sensitive to the relative doping levels in the $\delta$-doped peaks. Slightly asymmetric $\delta$-doping spikes are desired since the CB and valence band densities-of-states are not equal. Our calculations have shown that highly mismatched $p$- and $n$-$\delta$-doping spikes beyond this optimal ratio will result in a widened depletion width, consequently reducing $J_p$ by effectively increasing the tunneling distance. We effectively raised $J_p$ to 63 kA/cm$^2$ with an associated PVCR of 2.5 by increasing the P $\delta$-doping concentration to $3.4 \times 10^{14}$ cm$^{-2}$ while maintaining the B $\delta$-doping concentration at $1 \times 10^{14}$ cm$^{-2}$ in an RITD having a 3-nm spacer ($L_1 = 1$ nm/$L_2 = 2$ nm). Figure 3 presents the calculated band diagram of this Si/SiGe RITD at an applied bias of 0.4 V showing the CB longitudinal ($X_z$) and transverse ($X_{xy}$) valleys and heavy-hole (HH), light-hole (LH), and split-off-hole bands. The fundamental $X_z$, $X_{xy}$, LH, and HH states in the



FIG. 2. A series of isothermal curves, each for a 1-min rapid thermal anneal varying from 600 to 775 °C, indicating the measured Si/SiGe RITD $J_p$ and PVCR versus the tunnel spacer thickness.
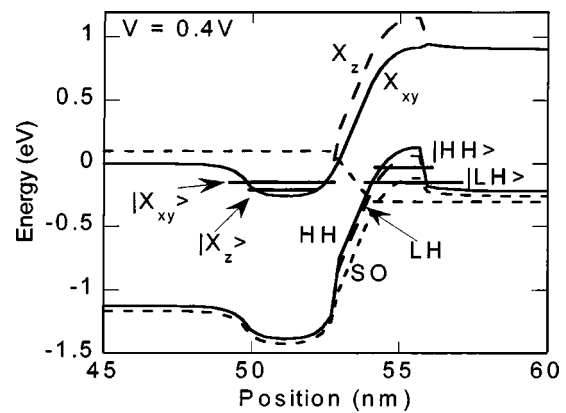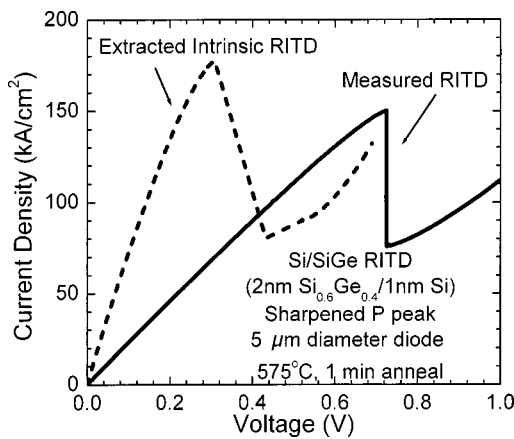
FIG. 4. Measured and extracted intrinsic $I-V$ characteristics of a 3-nm Si/SiGe RITD with elevated and sharpened P $\delta$-doping.
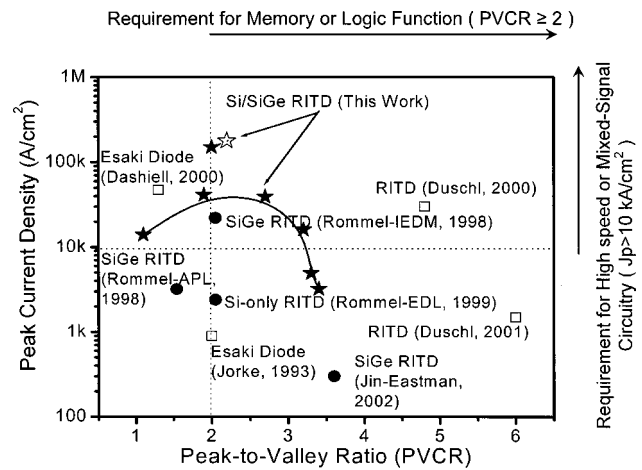


FIG. 5. A graph of PVCR plotted against the PCD of a number of Si-based interband tunnel diodes including those presented in this study. Data points from other research groups are shown as open squares, data from previous work by the authors is shown as solid circles, and data from this study is shown as stars (solid for measured data and open for extracted data).

quantum wells are shown. It is calculated by solving five independent single-band effective mass equations. The potential is calculated semiclassically. P $\delta$-doping of $3.4 \times 10^{14}$ cm$^{-2}$ is assumed spread out over 3 nm and the B $\delta$-doping of $1.0 \times 10^{14}$ cm$^{-2}$ is spread out over 2 nm.

Finally, to further increase $J_p$, another Si/SiGe RITD was developed using a sharpened P $\delta$-doping peak by dropping the substrate temperature momentarily following the growth of the P $\delta$-doping spike to reduce P segregation and then raising the substrate temperature to accentuate the quantum well by sweeping out excess bulk doping. The narrower $\delta$-doping peak should lead to better confinement in the quantum well. After 4 nm of growth at 250 °C, the growth is momentarily stopped and the substrate temperature increased to 450 °C before resuming growth of the final 100-nm P-doped $n^+$ contact layer. Because of the higher substrate temperature relative to the other $n^+$ contact layers, this layer may have a slightly lower concentration of dopants. This results in a measured $J_p$ of 151 kA/cm$^2$ with PVCR of 2.0, which corresponds to a $J_p - J_v$ of 76 kA/cm$^2$, as shown in Fig. 4. The 151 kA/cm$^2$ current density reported here is commensurate to a number of reports for III-V-based RTDs.[13]

The actual active diode area is less than the lithographic area used in these current density calculations, due to the undercut of the mesa isolation etching during wet etching of the mesa diode which would increase the true $J_p$ value by about 18% over the conservative value reported here. At the very high current densities measured here, the nominal series resistance can act to skew the shape of the $I-V$ characteristics. Thus, the real PVCR is estimated to be 2.2 at room temperature. The $I-V$ characteristics of this intrinsic RITD were extracted and plotted in Fig. 4 also adjusted for the mesa undercut and series resistance.

No area dependence on $J_p$ was observed in all our diodes. $J_p$ is very consistent while measuring diodes with different sized areas, which indicates that high current values can simply be obtained by increasing the diode area. Finally, Fig. 5 summarizes these results by plotting the PVCR against its corresponding $J_p$ for a number of previous Si-based interband tunnel diodes. The extremely high peak current density of 151 kA/cm$^2$ equates to an estimated speed index

equal to 34 mV/ps. This estimated speed index is substantially higher than previous speed index reports.[11,12,14]

In conclusion, our study shows peak current densities over 151 kA/cm$^2$ and PVCR greater than 2 in Si/SiGe resonant interband tunneling diodes at room temperature, which results in an estimated speed index of 34 mV/ps. This result demonstrates the high potential of this type of Si-based tunnel diode for mixed-signal and high power oscillator applications.

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