"p-on-n" Si interband tunnel diode grown by molecular beam epitaxy

K. D. Hobart[a] and P. E. Thompson
Naval Research Laboratory, Washington, DC 20375

S. L. Rommel, T. E. Dillon, and P. R. Berger
Department of Electrical Engineering, University of Delaware, Newark, Delaware 19716

D. S. Simons and P. H. Chi
National Institute of Standards and Technology, Gaithersburg, Maryland 20988

(Received 17 May 2000; accepted 13 November 2000)

Si interband tunnel diodes have been successfully fabricated by molecular beam epitaxy and room temperature peak-to-valley current ratios of 1.7 have been achieved. The diodes consist of opposing *n*- and *p*-type δ-doped injectors separated by an intrinsic Si spacer. A "*p*-on-*n*" configuration was achieved for the first time using a novel low temperature growth technique that exploits the strong surface segregation behavior of Sb, the *n*-type dopant, to produce sharp delta-doped profiles adjacent to the intrinsic Si spacer. © *2001 American Vacuum Society.* [DOI: 10.1116/1.1339011]

I. INTRODUCTION

Recently there has been significant activity pursuing room temperature operation of Si and SiGe interband tunnel diodes.[1–5] The devices are particularly attractive for integration with Si-based microelectronic circuits and continued progress has seen the peak-to-valley current ratio (PVCR) exceed 5. The structure first demonstrated by Rommel *et al.*[1] consists of diametrical *n*- and *p*-type δ-doped layers separated by a narrow intrinsic barrier layer with similarities to an Esaki tunnel diode. To date, these devices have been grown by molecular beam epitaxy (MBE) in an "*n*-on-*p*" configuration, i.e., with the *n*-type δ-doped layer grown *last* to avoid segregation of the dopant (either Sb or P) into the barrier layer even at the very low growth temperatures ($\leqslant$400 °C) commonly used. The *p*-type dopant B exhibits significantly less surface segregation and well controlled δ-doped profiles are routinely grown. To increase the versatility of these devices and produce complementary tunnel diode structures, a novel growth technique is reported here for the fabrication of "*p*-on-*n*" interband tunnel diodes. The technique exploits surface segregation properties of Sb during Si MBE growth to produce sharp δ-doped profiles adjacent to *and* preceding the intrinsic barrier layer.

Achieving sharp, arbitrary *n*-type doping profiles during Si and SiGe MBE is challenging and several approaches have been investigated to overcome the high surface segregation ratio of P, As, and Sb.[6] Such approaches include low temperature MBE,[7] "buildup," and "flash-off",[8] and *in situ* ion implantation.[9] Each has its limitations and for the latter technique it is one primarily of cost and complexity. Low temperature epitaxy (LTE) is a simple technique where the low growth temperature kinetically limits surface segregation processes. Film quality is however compromised in return for achieving active Sb doping levels in excess of $5\times10^{20}\,\mathrm{cm}^{-3}$. LTE is most useful for producing low resistance contact layers since these layers are typically grown last in the layer sequence and do not jeopardize the integrity of preceding layers. For the "*n*-on-*p*" tunnel diodes reported previously, sharp *n*-type δ-doping profiles are produced with LTE by interrupting growth, depositing a partial monolayer of either Sb or P, and resuming epitaxy. Surface segregation of *n*-type dopants decreases significantly at low temperature but still exists and leads to a significant segregation "tail" following growth of the δ-doped layer. Buildup and flash-off techniques were employed in the infancy of Si MBE and as the terms imply involve building up certain coverage of dopant on the surface during a growth interruption, growing a given Si film thickness, and finally raising the substrate temperature to desorb the excess dopant. The technique indeed produces sharp doping profiles although the high temperature step leads to undesirable dopant diffusion and constrains the maximum carrier concentration to solid solubility limits.[10] For the tunnel diodes described here minimizing diffusion is critical. The strong temperature dependence of the surface segregation ratio has been exploited to obtain sharp *n*-type δ-doped layers without the parasitic dopant tail. Figure 1 shows the measured surface segregation ratio *r* (ratio of surface N_{Surf} to bulk N_{Bulk} dopant concentrations) of Sb in Si as a function of growth temperature. It can be seen that the surface segregation can be manipulated over 320–550 °C for a potential four-orders-of-magnitude reduction in dopant incorporation. Additionally, there is a second effect that reduces the surface segregation ratio by up to a factor of 10: high dopant surface coverages reduce the surface free energy and the driving force for surface segregation, leading to the self-limiting segregation phenomenon.[11] This effect lowers the low temperature (<400 °C) portion of the curve in Fig. 1 by nearly ten times for surface concentrations exceeding $2-3\times10^{14}\,\mathrm{cm}^{-2}$.[7] In this work, these phenomena are exploited and low temperatures (320 °C) are employed to incorporate Sb into δ-doped layers. The dopant tail is virtually eliminated by cycling to moderate substrate temperatures (550 °C) that considerably reduce Sb incorporation, inducing residual dopant to "float" on the growing surface while simultaneously minimizing dopant diffusion.

[a]Electronic mail: hobart@nrl.navy.mil

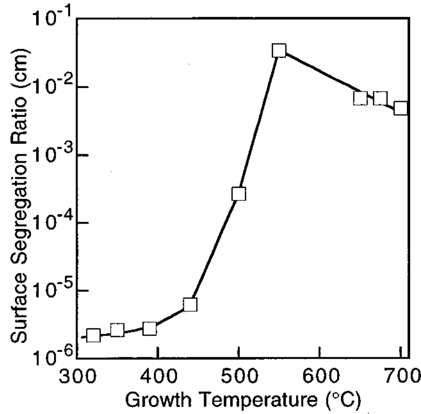

FIG. 1. Measured steady-state surface segregation ratio of Sb in Si as a function of growth temperature. The surface segregation ratio is defined as the ratio of surface to bulk dopant concentrations and the measured data are for dilute surface concentrations ($\leqslant 1\times 10^{14}\,\mathrm{cm}^{-2}$).

II. EXPERIMENT

The growths were performed in a MBE system equipped with solid source electron beam heated Si and Ge crucibles. Sb was evaporated from a conventional effusion cell and B from a high-temperature effusion cell. Growth temperature was controlled by a pyrometer and calibrated by Au–Si and Al–Si eutectic points. For all the growth experiments described below, 75 mm 0.01 Ω cm Sb-doped Si(100) wafers were used. All wafers were cleaned with an HF-last process[12] and immediately loaded into the vacuum chamber. A schematic cross section of the layer structure is shown in Fig. 2. Si buffer layer growth was initiated at 650 °C and a 10 nm buffer was grown at which point another 10 nm of Si was grown while the substrate temperature was ramped down to 450 °C. At this point growth was interrupted for the Sb δ doping. The temperature was lowered from 450 to 320 °C while $3\times 10^{14}\,\mathrm{cm}^{-2}$ Sb was deposited. Growth was resumed at 320 °C following Sb deposition and a thickness $L_1=2$ or 5 nm of Si was grown. The growth was again interrupted and the temperature increased to 550 °C at which point growth was resumed and a thickness $L_2=3$, 6, or 9 nm of Si was grown. Growth was then interrupted for B δ doping and $3\times 10^{14}\,\mathrm{cm}^{-2}$ B was deposited. Growth was resumed and an undoped 20 nm Si layer was grown followed by a 50 nm p^+ cap doped $1\times 10^{20}\,\mathrm{cm}^{-3}$. Portions of each wafer were given a 650 °C 60 s rapid thermal treatment that, in the past, has been shown to achieve the highest negative differential resistance (NDR).

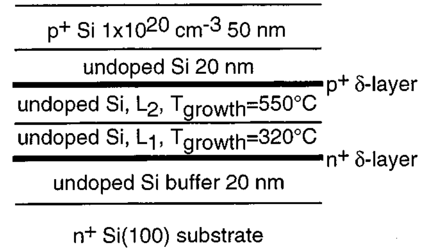

FIG. 2. Schematic cross section of the tunnel diode showing the MBE growth variables L_1 and L_2.

Simple mesas diodes were fabricated by first delineating circular Ti/Au contacts by lift-off lithography. The metal was also the self-aligned mask for subsequent plasma etching to isolate individual diodes with as-drawn diameters of 10, 18, and 50 μm. Backside Al provided contact to the n^+ substrate. Devices were characterized by current–voltage ($I-V$) measurements at room temperature. The dopant profiles were also characterized by secondary ion mass spectrometry (SIMS), using an O_2^+ ion beam with a primary impact energy of 3 keV at an incidence angle of 52° from normal.

III. RESULTS AND DISCUSSION

The strong increase in Sb surface segregation that is obtained by raising the substrate temperature from 320 to 550 °C provides a corresponding reduction in dopant incorporation and thus doping concentration. Figure 3 shows a comparison of several SIMS profiles of diode structures to illustrate the efficacy of the thermal cycling approach. The effect of the parameter L_1 can be seen by comparing the Sb profiles of two *p*-on-*n* tunnel diodes with $L_1=5$ nm and $L_2=3$ nm [Fig. 3(a)] and $L_1=2$ nm and $L_2=3$ nm [Fig. 3(b)].

TABLE I. Nominal layer specifications, measured δ-doping peak separation, integrated Sb and B δ-doping concentrations, peak tunnel current density, and peak-to-valley current ratio (PVCR) of tunnel diodes in this study. The measured δ-doping peak separation and integrated Sb and B δ-doping concentrations were averaged over two SIMS profiles except for sample No. 2/3 where only one run was performed. Measurement uncertainties are ± 1 nm for the peak separation, $\pm 20\%$ for the doping concentrations, and better than 1 part in 10^4 for the electrical measurements.

Sample No.	L_1 (nm)	L_2 (nm)	Measured peak separation (nm)	Measured Sb δ conc. $\times 10^{14}\,\mathrm{cm}^{-2}$	Measured B δ conc $\times 10^{14}\,\mathrm{cm}^{-2}$	Ave. peak current density (A/cm^2)	Ave. PVCR
2/3	2	3	4.0	0.82	2.5	2891	1.4
2/6	2	6	7.7	1.1	2.6	115	1.2
5/3	5	3	7.4	2.1	2.4	2569	1.7
5/6	5	6	9.7	1.8	2.5	15	1.2
5/9	5	9	13.8	2.4	2.4	<10	N/A

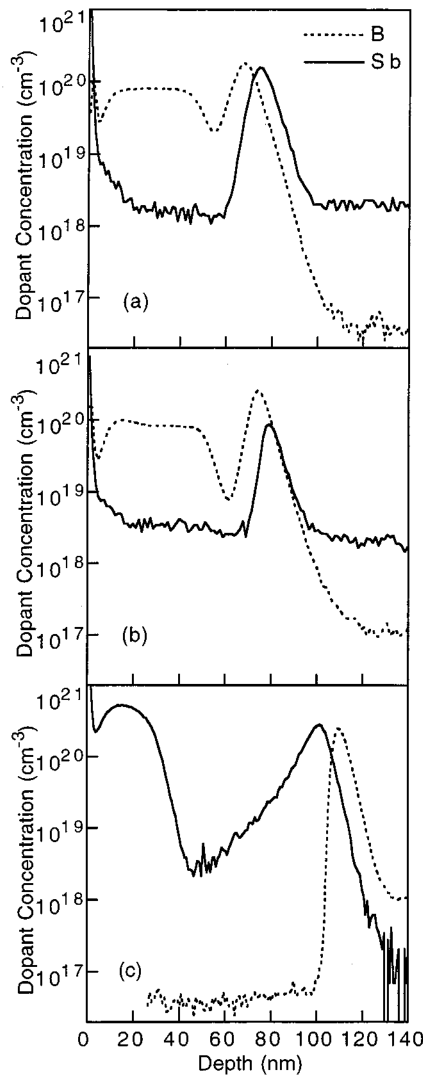

FIG. 3. SIMS profiles for two *p*-on-*n* tunnel diodes with: (a) $L_1=5$ nm and $L_2=3$ nm, (b) $L_1=2$ nm, and $L_2=3$ nm, and (c) a typical *n*-on-*p* tunnel diode with a 4 nm intrinsic spacer. Note the long decay length of the Sb profile in the *n*-on-*p* diode, grown at 320 °C, is all but absent in the *p*-on-*n* diodes.

Table I gives the layer parameters, the measured integrated dose of the Sb, and B δ-doping profiles, measured peak separation, and diode characteristics, which are discussed below. Figure 3 and Table I show that by increasing the parameter L_1 from 2 to 5 nm, the incorporation of Sb increases by approximately a factor of 2 and approaches the nominal dose ($3\times10^{14}\,\mathrm{cm}^{-2}$). The measured B δ dose is invariant as expected. Figure 3(c) is a typical *n*-on-*p* tunnel diode grown by LTE at a growth temperature of 320 °C and is shown to illustrate the improvement in abruptness of the Sb profile using the thermal cycling technique developed here. It can be seen that the broad tail is eliminated. Quantitative assessment of the profile abruptness using SIMS is difficult. Even for the conditions used here, SIMS-induced broadening masks the true δ-doping profiles which are known to be much sharper than shown in Fig. 3.

The actual Sb doping concentration can be predicted from

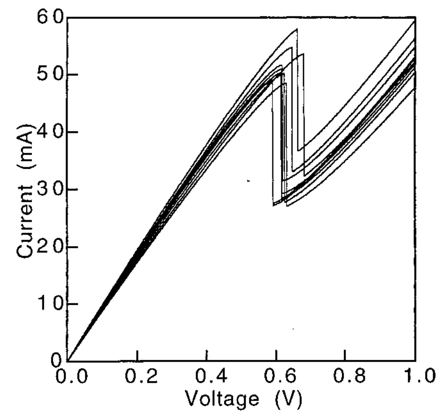

FIG. 4. Forward $I-V$ characteristics from ten diodes fabricated from sample No. 5/3. The diode diameter was 50 μm.

the known surface segregation ratio. The estimated dopant concentration is the ratio of the Sb δ dose to the surface segregation ratio. The actual surface segregation ratio is a nonlinear function of the dopant surface concentration above surface concentrations of $2\times10^{13}\,\mathrm{cm}^{-2}$, the relevant regime for the epitaxial growth of these devices. A detailed analysis of the surface segregation ratio was previously performed by the authors.[7] For the growth conditions in this study ($N_{\mathrm{Surf,Sb}}=3\times10^{14}\,\mathrm{cm}^{-2}$) the surface segregation ratio *r*, at a growth temperature of 320 °C, is approximately 5×10^{-7} cm leading to a bulk concentration $N_{\mathrm{Bulk,Sb}}$ of $6\times10^{20}\,\mathrm{cm}^{-3}$. The surface segregation ratio also represents the approximate thickness of Si required to incorporate most of the δ Sb dose, and explains why the profiles with $L_1=5$ nm have measured Sb doses close to the nominal deposited dose.

The variation in the above profiles had a strong effect on the electrical performance of the tunnel diodes. The $I-V$ characteristics of ten diodes from sample No. 5/3 are shown in Fig. 4, illustrating good uniformity in the NDR characteristics. The peak voltage (i.e., the voltage at which the NDR peak occurs) is shifted to higher voltage than is expected due to the combination of high series resistance and high peak current density J_P. Table I gives the peak current density and PVCR averaged over at least ten diodes. In these diodes the magnitude of the peak tunnel current density J_P is affected by two primary components:[13] (1) the degenerate electron and hole concentration *N*, ($J_P\sim\exp(-N^{-1/2})$) and (2) the spatial separation *w* of the degenerate doping peaks ($J_P\sim\exp(-w)$). This is illustrated by the high peak current densities of sample Nos. 2/3 and 5/3, where the former has a narrow peak separation and lower doping concentration and in the latter the situation is reversed. In all other cases the peak current density falls off rapidly and finally for sample No. 5/9 no NDR is observable and the $I-V$ characteristic is typical of a "backward" diode. The PVCR behavior is more difficult to predict but it is clear that the diodes with higher peak current density also have higher PVCR. The highest PVCR observed for any of the diodes fabricated here was

approximately 2 (No. 5/3) and represents a significant advancement towards realizing complementary tunnel diode devices.

IV. SUMMARY

Si *p*-on-*n* interband tunnel diodes have been grown for the first time by MBE by exploiting the strong temperature dependence of the Sb surface segregation ratio. A thermal cycling technique was successfully developed that produced tunnel diodes with PVCR of 1.7 and peak current density of nearly 3 kA/cm^2. It is expected that further improvements in the structure will push the PVCR up to that presently obtained with *n*-on-*p* diode configurations.

[1]S. L. Rommel *et al.*, Appl. Phys. Lett. **73**, 2191 (1998).
[2]S. L. Rommel, T. E. Dillon, P. R. Berger, P. E. Thompson, K. D. Hobart, R. Lake, and A. C. Seabaugh, IEEE Electron Device Lett. **20**, 329 (1999).
[3]R. Duschl, O. G. Schmidt, G. Reitemann, E. Kasper, and K. Eberl, Electron. Lett. **35**, 1111 (1999).
[4]P. E. Thompson *et al.*, Appl. Phys. Lett. **75**, 1308 (1999).
[5]R. Duschl, O. G. Schmidt, and K. Eberl, Appl. Phys. Lett. **76**, 879 (2000).
[6]K. D. Hobart, F. J. Kub, G. G. Jernigan, and P. E. Thompson, J. Vac. Sci. Technol. B **14**, 2229 (1996).
[7]K. D. Hobart, D. J. Godbey, M. E. Twigg, M. Fatemi, P. E. Thompson, and D. S. Simons, Surf. Sci. **334**, 29 (1995).
[8]S. S. Iyer, R. A. Metzger, and F. G. Allen, J. Appl. Phys. **52**, 5608 (1981).
[9]J.-P. Noël, J. E. Greene, N. L. Rowell, and D. C. Houghton, Appl. Phys. Lett. **56**, 265 (1990).
[10]K. D. Hobart, D. J. Godbey, P. E. Thompson, and D. S. Simons, J. Vac. Sci. Technol. B **11**, 1115 (1993).
[11]S. Fukatsu, K. Fujita, H. Yaguchi, Y. Shiraki, and R. Ito, Appl. Phys. Lett. **59**, 2103 (1991).
[12]P. E. Thompson, M. E. Twigg, D. J. Godbey, K. D. Hobart, and D. S. Simons, J. Vac. Sci. Technol. B **11**, 1077 (1993).
[13]S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981), pp. 520–530.