ELSEVIER

Thin Solid Films 380 (2000) 145–150

thin solid films

www.elsevier.com/locate/tsf

Epitaxial Si-based tunnel diodes

P.E. Thompson[a,*], K.D. Hobart[a], M.E. Twigg[a], S.L. Rommel[b], N. Jin[b], P.R. Berger[b], R. Lake[c], A.C. Seabaugh[d], P.H. Chi[e], D.S. Simons[e]

[a]*Naval Research Laboratory, Washington, DC 20375-5347, USA*
[b]*Department of Electrical and Computer Engineering, University of Delaware, Newark, DE 19716, USA*
[c]*Applied Research Laboratory, Raytheon Systems Company, Dallas, TX 75243, USA*
[d]*Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556, USA*
[e]*National Institute of Standards and Technology, Gaithersburg, MD 20899, USA*

Abstract

Tunneling devices in combination with transistors offer a way to extend the performance of existing technologies by increasing circuit speed and decreasing static power dissipation. We have investigated Si-based tunnel diodes grown using molecular beam epitaxy (MBE). The basic structure is a p^+ layer formed by B delta doping, an undoped spacer layer, and an n^+ layer formed by Sb delta doping. In the n-on-p configuration, low temperature epitaxy (300–370°C) was used to minimize the effect of dopant segregation and diffusion. In the p-on-n configuration, a combination of growth temperatures from 320 to 550°C was used to exploit the Sb segregation to obtain a low Sb concentration in the B-doped layer. Post-growth rapid thermal anneals for 1 min in the temperature interval between 600 and 825°C were required to optimize the device characteristics. J_p, the peak current density, and the peak-to-valley current ratio (PVCR), were measured at room temperature. An n-on-p diode having a spacer layer composed of 4 nm $Si_{0.6}Ge_{0.4}$, bounded on either side by 1 nm Si, had a $J_p = 2.3$ kA/cm^2 and PVCR = 2.05. A p-on-n tunnel diode with an 8 nm Si spacer (5 nm grown at 320°C, 3 nm grown at 550°C) had a $J_p = 2.6$ kA/cm^2 and PVCR = 1.7.

Keywords: Tunnel diodes; Epitaxy; Delta doping; Silicon; Silicon–germanium

1. Introduction

Since tunnel diodes were first reported by Esaki [1], there have been numerous attempts to exploit their intrinsically fast switching speed and negative differential resistance (NDR) in circuits to increase speed, reduce standby current, and minimize device count. For example, it has been demonstrated that a standard six transistor complementary metal oxide Si (CMOS) static random access memory (SRAM) cell could be replaced with a cell composed of one transistor, a capacitor, and two tunnel diodes, reducing the device area by a factor of 2.2 and decreasing the standby current by a factor of 8 [2]. Progress in this area has been limited by two primary factors. While Si Esaki tunnel diodes, based on a degenerately doped p/n junction, have reported peak-to-valley current ratios (PVCR) > 4, the lack of an epitaxial formation process prevents easy integration with CMOS. The second factor is low PVCR in Si tunnel diode configurations which are integrable with CMOS. The band offsets between Si and $Si_{1-x}Ge_x$ are inadequate for significant room temperature NDR in a resonant tunnel diode (RTD). Hole RTDs have not been reported to have NDR above a temperature of 77 K [3–8]. The electron RTD reported by Ismail [9] had a PVCR of 1.2 at 300 K, but a thick (> 1 μm) relaxed SiGe buffer layer is

* Corresponding author. Tel.: +1-202-404-8541; fax: +1-202-404-7194.
E-mail address: thompson@estd.nrl.navy.mil (P.E. Thompson).

0040-6090/00/$ - see front matter
PII: S0040-6090(00)01490-5

required to place the Si barrier layer under strain to produce sufficient conduction band offset. The most promising epitaxial Si tunnel diode was reported by Jorke [10], which was a Si p^+-*i*-n^+ junction, which resulted in a PVCR of 2 and a peak current density of 0.8 kA/cm^2. Sweeney and Xu [11] have proposed a resonant interband tunnel diode (RITD) structure, which combines the structure and behavior of both RTDs and Esaki diodes. The RITD is a double-well bipolar device, in which electrons in the n-type two-dimensional quantum well resonantly tunnel through a barrier layer into the p-type quantum well, and vice versa [11]. In our work, we have used the Sweeny and Xu configuration, forming the two-dimensional quantum wells in Si by B and Sb delta doping and the barrier layer with a combination of Si and $Si_{1-x}Ge_x$, to develop high performance, epitaxial Si tunnel diodes.

2. Experimental

The Si-based RITDs were grown using solid source MBE. Si and Ge were deposited by e-beam evaporation. The dopants, B and Sb, were obtained by evaporation of elemental sources in Knudsen cells. The substrate temperature during growth was monitored by an optical pyrometer which was calibrated by observing the eutectic temperatures of Au/Si (363°C) and Al/Si (577°C) on equivalent substrates. Prior to device fabrication, portions of the samples were annealed to improve the device characteristics. Rapid thermal annealing (RTA) was employed using temperatures from 575 to 825°C. Atomic concentration profiles were obtained by secondary ion mass spectrometry (SIMS) using a high-performance magnetic sector secondary ion mass spectrometer. The net impact energy of the primary beam, 3 keV O_2^+, was selected in order to minimize profile broadening by ion beam mixing. Depth scales were obtained from stylus profilometry ($\pm 3\%$ uncertainty). The atomic carrier concentrations of B and Sb were calibrated with implant standards ($\pm 20\%$ uncertainty in integrated area density).

3. Sb and B delta doping

Since Sb and B delta doping are fundamental to the structure of the RITD, a thorough investigation has been made into the activation and spatial distribution of the dopants. Doping of Si with Sb is problematic because of Sb's large surface segregation ratio, which is defined as the Sb surface coverage, normalized to the number of Si(100) surface sites (6.8×10^{14}/cm^2), divided by the bulk Sb fraction, which is the Sb bulk doping concentration normalized to the atomic density of Si [12]. It has been shown previously [13,14] that the segregation of Sb in Si can be reduced by more than four orders of magnitude by lowering the surface temperature during growth from 550 to 320°C. Epitaxial growth can still be maintained at 320°C as long as a critical thickness for a specific growth-rate is not exceeded. For a growth-rate of 0.1 nm/s and a substrate temperature of 320°C, the critical thickness is approximately 120 nm [15,16]. To investigate Sb delta doping at 320°C, a Sb delta layer was grown on a Si(100) p-type (10–20 Ω/cm) wafer between a thick undoped Si buffer layer and a 30-nm undoped Si cap. Portions of the wafer were furnace annealed for 10 min in a N_2 atmosphere at temperatures of 500, 600, 700, or 800°C or were rapid thermal annealed for 10 s in a N_2 atmosphere in the same interval of temperatures. Room temperature Hall measurements were performed on three or four samples from each annealed condition and on as-grown samples. SIMS was also done on a representative sample from each anneal condition and on an as-grown sample. The results are shown in Fig. 1a,b. When the as-grown sheet carrier concentration is compared to the sheet Sb concentration, which is obtained by integrating the SIMS atomic concentration profile with respect to depth, the activation of the Sb was 100% if a Hall factor of 1.5 was used. We have used this value for the Hall factor in the evaluation of the annealed samples. It is observed in Fig. 1a that the

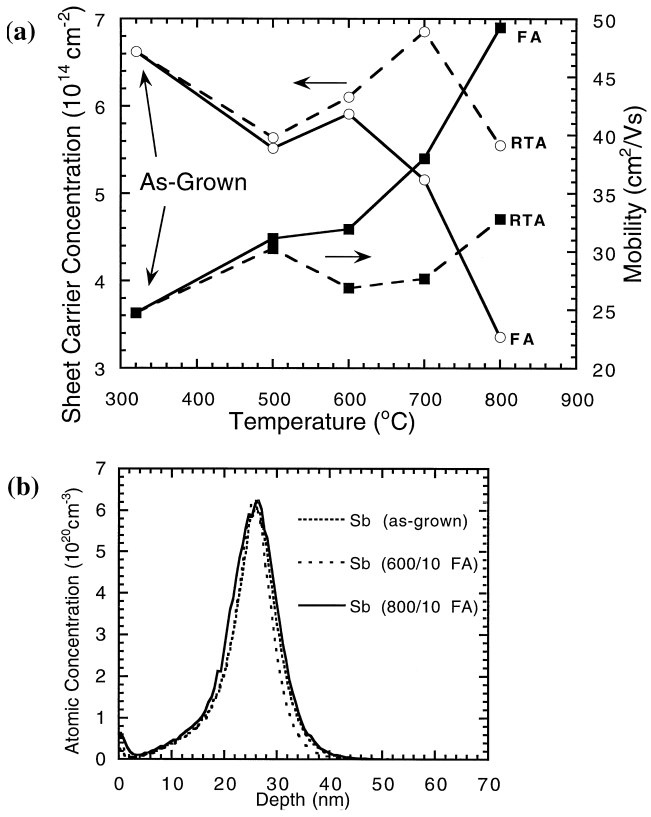

Fig. 1. (a) Hall measurements of Sb delta-doped Si grown at 320°C and annealed at 500, 600, 700 and 800°C. (b) SIMS atomic concentration profile of Sb delta-doped Si as-grown at 320°C and after 10 min FA at 600 and 800°C.

annealed samples [both furnace annealed (FA) and RTA] have a maximum carrier concentration between 600 and 700°C and the mobility increased for anneals from 600 to 800°C. Unfortunately, variation of the Hall factor by the anneal affects both the measured values of concentrations and mobilities. However, the sheet resistance, which is not affected by the Hall factor, shows a pronounced minimum at 700°C for both RTA and FA. We observe some redistribution of the Sb after anneal (Fig. 1b). After a 10-min 800°C FA the full width-half maximum of the SIMS atomic concentration profile has increased to 10.4 nm from 8.6 nm.

B delta doping was investigated in a similar manner. The initial experiment determined the maximum sheet concentration of B in the delta-doped layer, which was fully electrically active. Again choosing a growth temperature of 320°C to minimize dopant diffusion during growth, B delta-doped layers having a dopant sheet concentration of $10^{14}/cm^2$, $3\times10^{14}/cm^2$, and $5\times10^{14}/cm^2$ were deposited and covered with a 10-nm Si cap. The Hall measurements revealed a linear increase in the carrier concentration with B concentration for sheet concentrations up to $3\times10^{14}/cm^2$. The anneal characteristics of a second set of samples, each having a B delta-doped layer of $3\times10^{14}/cm^2$ covered with a 30-nm Si cap, were measured. A Hall factor of 0.6 was used to make the Hall measurements compatible with the integrated B atomic profiles obtained by SIMS. This value for the Hall factor is consistent with values used by other researchers investigating heavily B-doped Si [17]. The carrier concentration and mobility for samples which have undergone either a 10-min FA or a 10-s RTA are plotted in Fig. 2a. As with the Sb delta-doped samples, variation in the Hall factor with anneal may mask changes in the carrier concentration and mobility. Assuming that the Hall factor does not change, the carrier concentration variation is less than 10% about its average value, and may be accounted for by doping non-uniformity. The twofold increase in the mobility with anneal from 600 to 800°C is significant. The mobility increase is due to the reduction of point defects and to the diffusion of B, Fig. 2b, which reduces the average ionized impurity scattering. The key results from the Sb and B delta doping investigation were used to design the structures of the RITD and explain the diode characteristics.

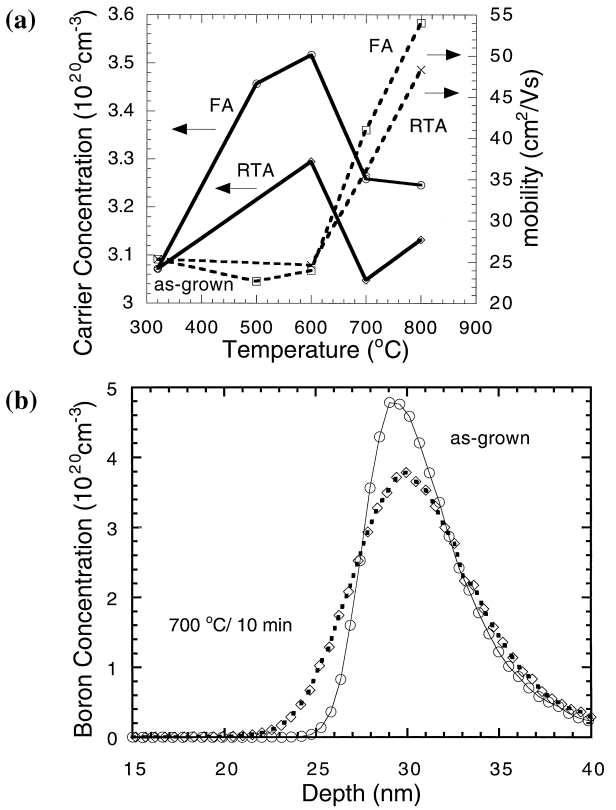

Fig. 2. (a) Hall measurements of B delta-doped Si grown at 320°C and annealed at 500, 600, 700 and 800°C. (b) SIMS atomic concentration profiles of B delta-doped Si, as-grown at 320°C and after a 10-min FA at 700°C.

4. $Si_{1-x}Ge_x$ RITD

4.1. Review of previous work

We initially reported a $Si/Si_{0.5}Ge_{0.5}$ RITD with a PVCR of 1.54 at a peak current density of 3.2 kA/cm^2 [18]. The configuration was a p^+ Si substrate, 100 nm p^+ Si (B-doped $2\times10^{19}/cm^3$), B delta-doped layer ($7\times10^{13}/cm^2$), 1 nm Si spacer, 4 nm $Si_{0.5}Ge_{0.5}$, 1 nm Si spacer, Sb delta-doped layer ($3\times10^{14}/cm^2$), and n^+ Si (Sb-doped $4\times10^{19}/cm^3$). In order to obtain NDR we grew most of the structure at 370°C and followed with a 1-min RTA at 700°C. An equivalent structure was grown with only Si spacers (2 or 4 nm) between the delta-doped layers and the PVCR/peak current densities were 1.45/9.4 and 1.38/1.36 kA/cm^2, respectively [19]. By lowering the substrate temperature during growth to 320°C, increasing the doping in the p^+ delta layer to $3\times10^{14}/cm^2$, and placing undoped layers surrounding the delta-doping planes, we were able to fabricate Si RITDs with an average PVCR of 2.05 with a peak current density of 2.4 kA/cm^2 [20]. The Si RITD required a post-growth 1 min RTA between 600 and 625°C to achieve optimum performance. Duschl and colleagues [21,22] have investigated similar structures followed by the post-growth anneal, but used P as the n-type dopant and have obtained impressive results of 5.45 PVCR and 8 kA/cm^2 peak current density.

4.2. SiGe RITD with sharper Sb delta-doped layers

We have attempted to improve our device results by making adjustments to our structure to reduce the valley current while maintaining the peak current. The

new structure is as follows: The B concentration in the p^+ layer was $5 \times 10^{19}/cm^3$, grown at 500°C and the B delta-doping was $1 \times 10^{14}/cm^2$, during which the temperature was reduced to 320°C. The undoped spacer configuration was 1 nm Si, 4 nm $Si_{0.6}Ge_{0.4}$, and 1 nm Si, all grown at 320°C. The Sb delta doping was $1 \times 10^{14}/cm^2$, during which temperature was lowered from 320 to 250°C in an attempt to compensate for the higher segregation ratio of Sb compared to P [23]. We further sharpened the Sb n^+ doping spike by growing 4 nm of Si at 250°C with the Sb shutter closed, doping the Si with the segregating Sb. Then the temperature was raised to 350°C to increase the Sb segregation, reducing the Sb incorporation. The Sb shutter was opened and a 100-nm n^+ layer having a concentration of $3 \times 10^{19}/cm^3$ was grown. The structure is shown in Fig. 3a and a high resolution transmission electron micrograph of the delta-doped region of the as-grown sample is represented in Fig. 3b. It is observed that the sample is still crystalline, even though portions were grown at a temperature of 250°C. The as-grown sample did not have NDR. Portions of the wafer were annealed for 1 min at temperatures from 650 to 825°C. The current–voltage curves are shown in Fig. 4a and the peak and valley current densities and PVCR as a function of anneal temperature are represented in Fig. 4b. It is observed that the maximum PVCR is still only slightly greater than two in spite of our efforts to make the Sb doping spike sharper.

The anneal characteristics of our Sb-doped RITDs, as shown in Fig. 4b, are consistently different than the anneal characteristics reported for the P-doped tunnel diodes [21]. For example, in Fig. 4b the peak current

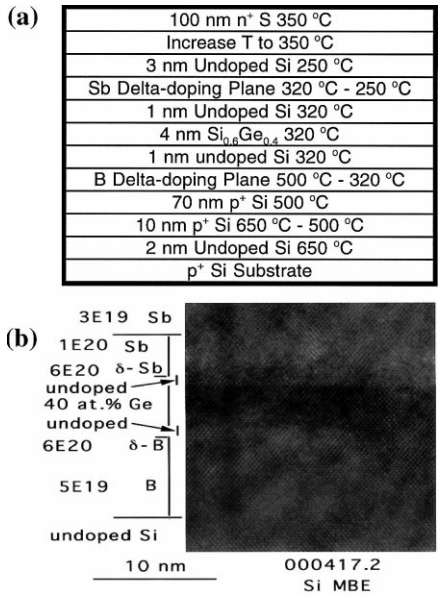

Fig. 3. (a) Schematic of SiGe RITD designed with sharper Sb delta-doped layer. (b) HRTEM micrograph of the SiGe RITD, schematic in 3a.

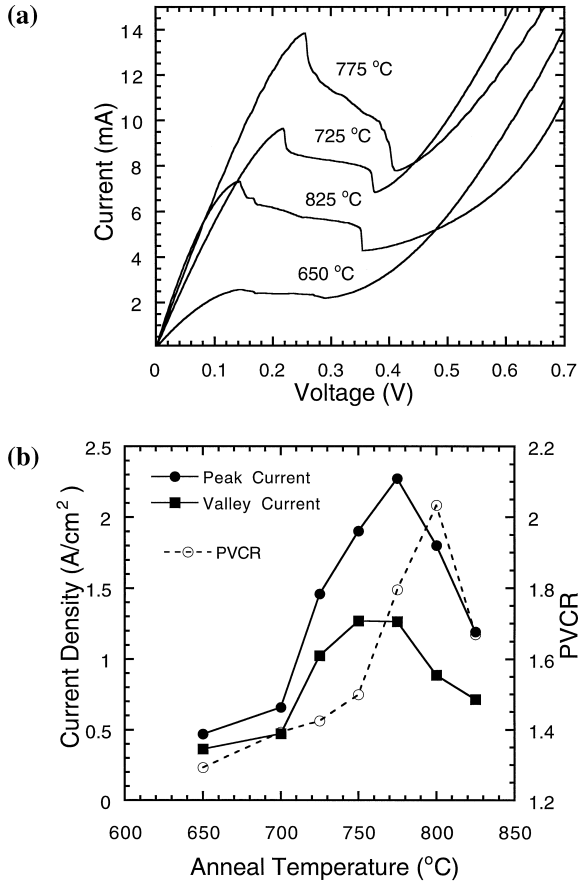

Fig. 4. (a) I–V of the SiGe RITD after 1 min RTA. (b) Peak and valley current density and PVCR as a function the RTA anneal temperature.

density increased with anneal temperature up to a maximum and then decreased with higher anneal temperatures. The valley current density followed the temperature trend of the peak current. The maximum in PVCR was observed after the 800°C RTA. However, the peak current of the P-doped tunnel diodes remains almost constant at temperatures up to 680°C, while the valley current shows substantial decrease [21]. At temperatures higher than 680°C, both the peak and valley currents decrease. The decrease in the peak with high temperature anneal observed in both Sb- and P-based diodes is due to dopant diffusion (see Fig. 2b) increasing the width of the depletion layer and, therefore, reducing the tunneling probability. The explanation for the low temperature anneal behavior of the valley current in P-doped tunnel diodes is the reduction of point defects formed during the low temperature MBE growth [22]. The question remains: Why do the peak currents in the Sb-doped RITD increase with anneal temperature? Between 650 and 775°C, the peak current has increased by a factor of 5. From the activation studies presented above, there does not seem to be a sufficient increase in the dopant concentrations to account for the increase in current. We have attempted

numerous growth schemes, such as increasing the substrate temperature during the growth of the region between the delta-doped layers, to change the point defect concentration, but observed no improvement in device performance. There is one difference between Sb and P that cannot be ignored: Sb is a much larger atom. An Sb concentration of $1 \times 10^{20}/\text{cm}^3$ in Si results in a strained layer with an excess lattice parameter of 10^{-4} nm [14]. At this point we can only speculate that the strain in the as-grown Sb delta-doped layer and its change during anneal may affect the tunnel and excess currents.

4.3. p-on-n Si RITD

In order to easily incorporate the RITD into a circuit, it is necessary to have a p-on-n configuration as well as an n-on-p. The concern is how to deposit the Sb first and not have the segregating Sb component interfere with either the undoped spacer layer or the B doping layers. We have chosen to exploit the temperature sensitivity of the Sb segregation to keep the Sb concentration low in those regions. After the growth of a thin buffer layer at 650°C on an n^+ Si(100) substrate, the temperature was dropped to 320°C for the deposition of the Sb delta-doped layer. Keeping the substrate temperature at 320°C, but with the Sb shutter closed, a layer L1 was grown to incorporate the segregating Sb. Then, the substrate temperature was raised to 550°C, at which temperature the segregation ratio of Sb increased by four orders of magnitude and a second undoped Si layer, L2, was grown. Finally the B delta-doped layer and the p^+ contact layer were grown, all at 550°C. Complete details of this work may be found elsewhere [24]. The SIMS atomic profile of a structure with L1 and L2 equal to 5 and 3 nm, respectively, and the current–voltage curve are represented in Fig. 5a,b. NDR was observed in the unannealed samples. The maximum PVCR of 2.0 was observed after a 575°C, 1-min RTA, and the peak current density was 1.6 kA/cm^2. The maximum peak current density of 2.6 kA/cm^2 was observed after a 650°C, 1-min RTA and the PVCR was 1.7.

5. Summary

Si-based RITD were fabricated using Sb and B delta doping and a Si or Si/SiGe/Si spacer layer. A post-growth RTA between 600 and 800°C was required for optimum device performance. The effect of the anneal on device current–voltage characteristics was substantially different for the Sb-based tunnel diodes compared to P-based tunnel diodes. Both the peak current, which is the tunnel current, and the valley current increased with anneal temperature until device performance was eroded by impurity diffusion. By exploiting the segregation of Sb, we were able to fabricate a p-on-n tunnel diode to complement the n-on-p structures.

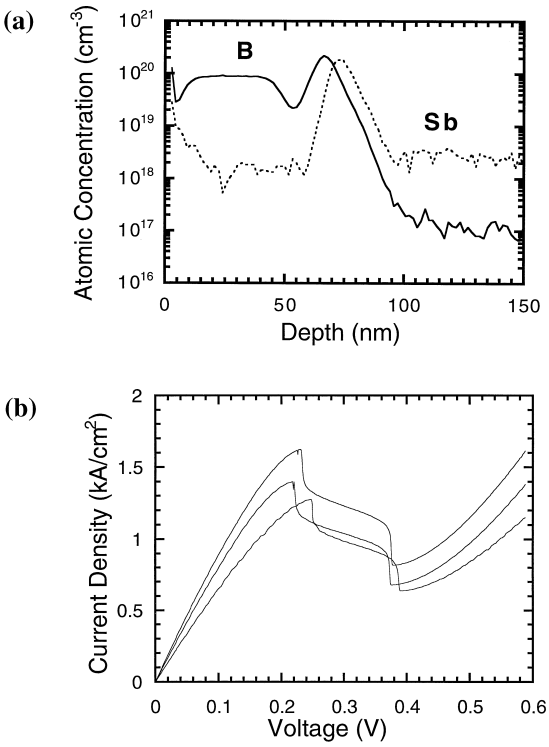

Fig. 5. (a) SIMS atomic concentration profile of p-on-n RITD with L1 = 5 nm and L2 = 3 nm. (b) I–V curves of four adjacent diodes having a diameter of 50 μm after a 575°C, 1-min RTA.

Acknowledgements

This work was supported by the Office of Naval Research, National Science Foundation, and Defense Advanced Research Projects Agency. The authors thank Lt. Col. Gernot Pomrenke for his encouragement throughout the project.

References

[1] L. Esaki, Phys. Rev. 109 (1958) 603.
[2] A. Seabaugh, X. Deng, T. Blake, B. Brar, T. Broekaert, R. Lake, F. Morris, G. Frazier, IEDM Tech. Digest. 98 (1998) 429.
[3] H.C. Liu, D. Landheer, M. Buchanan, D.C. Houghton, Appl. Phys. Lett. 52 (1988) 1809.
[4] S.S. Rhee, J.S. Park, R.P.G. Karunasiri, Q. Ye, K.L. Wang, Appl. Phys. Lett. 53 (1988) 204.
[5] E. Kasper, H. Dambkes, J.-F. Luy, IEDM Tech. Digest. 1988 (1988) 558.
[6] U. Konig, M. Kuisl, J.-F. Luy, F. Schaffler, Electron. Lett. 25 (1989) 1169.
[7] U. Gennser, V.P. Kesan, S.S. Iyer, T. Bucelot, E. Yang, J. Vac. Sci. Technol. B8 (1990) 210.
[8] A. Zaslavsky, D.A. Grutzmacher, Y.H. Lee, W. Ziegler, T.O. Sedgwick, Appl. Phys. Lett. 61 (1992) 2872.
[9] K. Ismail, B.S. Myerson, P.J. Wang, Appl. Phys. Lett. 59 (1991) 973.

[10] H. Jorke, H. Kibbel, K. Strohm, E. Kasper, Appl. Phys. Lett. 63 (1993) 2408.
[11] M. Sweeny, J. Xu, Appl. Phys. Lett. 54 (1989) 546.
[12] S.A. Barnett, J.E. Greene, Surf. Sci. 151 (1985) 67.
[13] H. Jorke, Surf. Sci. 193 (1988) 569.
[14] K.D. Hobart, D.J. Godbey, M.E. Twigg, M. Fatemi, P.E. Thompson, D.S. Simons, Surf. Sci. 334 (1995) 29.
[15] H. Jorke, H.-J. Herzog, H. Kibbel, Phys. Rev. B. 40 (1989) 2005.
[16] D.J. Eaglesham, H.-J. Gossmann, M. Cerullo, Phys. Rev. Lett. 65 (1990) 1227.
[17] Y. Sasaki, K. Itoh, E. Inoue, S. Kishi, T. Mitsuishi, Solid-State Electron. 31 (1988) 5.
[18] S.L. Rommel, T.E. Dillon, M.W. Dashiell, H. Feng, J. Kolodzey, P.R. Berger, P.E. Thompson, K.D. Hobart, R. Lake, A. Seabaugh, G. Klimeck, D. Banks, Appl. Phys. Lett. 73 (1998) 2191.
[19] S.L. Rommel, T.E. Dillon, P. Berger, P.E. Thompson, K.D. Hobart, R. Lake, A.C. Seabaugh, IEEE Electron. Device Lett. 20 (1999) 329.
[20] P.E. Thompson, K.D. Hobart, M.E. Twigg, G.G. Jernigan, T.E. Dillon, S.L. Rommel, P.R. Berger, D.S. Simons, P.H. Chi, R. Lake, A.C. Seabaugh, Appl. Phys. Lett. 75 (1999) 1308.
[21] R. Duschl, O.G. Schmidt, G. Reitemann, E. Kasper, K. Eberl, Electron. Lett. 35 (1999) 1.
[22] R. Duschl, O.G. Schmidt, K. Eberl, Appl. Phys. Lett. 76 (2000) 879.
[23] E. Freiss, J. Nutzel, G. Abstreiter, Appl. Phys. Lett. 60 (1992) 2237.
[24] K.D. Hobart, P.E. Thompson, S.L. Rommel, T.E. Dillon, P.R. Berger, D.S. Simons, P.H. Chi, to be published.