Si resonant interband tunnel diodes grown by low-temperature molecular-beam epitaxy

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(Received 20 April 1999; accepted for publication 2 July 1999)

Si resonant interband tunnel diodes that demonstrate negative differential resistance at room temperature, with peak-to-valley current ratios greater than 2, are presented. The structures were grown using low-temperature (320 °C) molecular-beam epitaxy followed by a postgrowth anneal. After a 650 °C, 1 min rapid thermal anneal, the average peak-to-valley current ratio was 2.05 for a set of seven adjacent diodes. The atomic distribution profiles of the as-grown and annealed structures were obtained by secondary ion mass spectrometry. Based on these measurements, the band structure was modeled and current–voltage trends were predicted. These diodes are compatible with transistor integration. © *1999 American Institute of Physics.*
[S0003-6951(99)01935-X]

There is current interest in tunnel diodes, which have characteristics very useful to the circuit designer for applications such as embedded memory and signal processing. Recent review articles[1–3] discuss potential applications of this family of devices in Si. The first tunnel diode, the Esaki diode,[4] which is an intrinsically simple device consisting of a degenerately doped p/n junction, has not found wide use in integrated circuits because of the lack of an epitaxial formation process. Epitaxial processes have been used for Si-based resonant tunnel diodes (RTD), which have demonstrated hole tunneling,[5–10] where the layers are grown on a Si substrate such that the Si barriers are relaxed and the SiGe well layer is compressively strained, and electron tunneling,[11,12] where the barrier layers are relaxed SiGe and the Si well layer is under tensile stress. None of the hole RTDs have reported negative differential resistance (NDR) above a temperature of 77 K, which severely restricts the range of their application. The electron RTD reported by Ismail[11] had a peak-to-valley current ratio (PVCR) of 1.2 at 300 K, while the device reported by Matutinovic-Krstelj[12] only had NDR at temperatures less than 220 K. Additionally, the electron RTDs are not compatible with complimentary metal oxide silicon (CMOS) or heterojunction bipolar transistor (HBT) integration since they require a thick (>1 μm) relaxed SiGe buffer layer. A recent device reported by Sardela[13] employing B δ-doped layers in Si had NDR at room temperature, with a PVCR of 1.1 and a peak current density of 4.8×10^3 A/cm^2. The exciting feature of the B δ-doped device is that the structure is compatible with CMOS and HBT integration, although the PVCR must be increased for the device to be useful. The search, then, is for a Si-based tunnel diode which has improved electrical characteristics and which is compatible with transistor integration.

In our initial study[14,15] we investigated SiGe resonant interband tunnel diodes (RITD), similar to RITD embodiment originally proposed by Sweeney and Xu.[16] By using low-temperature (370 °C) molecular-beam epitaxy (MBE), we were able to fabricate Si/$Si_{0.5}Ge_{0.5}$ RITDs having, at room temperature, a PVCR of 2.05. By replacing the $Si_{0.5}Ge_{0.5}$ with Si, we were able to produce a Si tunnel diode having a PVCR of 1.41.[15,17] The performance of the tunnel diodes was found to depend strongly on the δ-doping spacing and on the postgrowth annealing conditions. In this letter, we will demonstrate Si RITDs which have PVCR values greater than 2 without the added complexity of Ge.

The Si RITDs were grown on a 75 mm Si (100) B-doped (0.015–0.04 Ω cm) substrate using solid-source MBE. Prior to entry into the specially designed MBE growth system,[18] the Si substrate was cleaned using a procedure previously described,[19] which resulted in a stable, hydrogen-terminated surface. Si was deposited by e-beam evaporation. The dopants, B and Sb, were obtained by evaporation of elemental sources in Knudsen cells. The substrate temperature during growth was monitored by an optical pyrometer which was calibrated by observing the eutectic temperatures of Au/Si (363 °C) and Al/Si (577 °C) on equivalent substrates.

The device structure employed in this study is shown in Fig. 1. The key features of the growth which differentiate this from earlier structures are: (1) lower substrate temperature (320 °C) during growth, which was employed to minimize the segregation of the dopants; (2) increased doping in the $p^+\delta$ layer; and (3) undoped layers surrounding the

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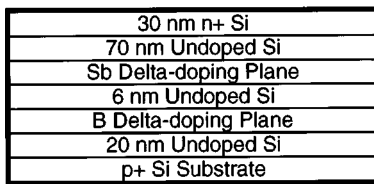

FIG. 1. Schematic diagram of the nominal Si RITD structure.

δ-doped planes to enhance carrier confinement. Growth was initiated at 650 °C to ensure removal of the hydrogen surface termination. After the growth of 10 nm of undoped Si, the substrate temperature was reduced to 450 °C while an additional 10 nm layer of undoped Si was grown. Si growth was interrupted and, concurrent with the deposition of B ($3\times10^{14}/\mathrm{cm}^2$) in a δ-doped layer, the temperature of the substrate was further reduced to 320 °C, which was the final temperature of the substrate during the remainder of the growth. A 6 nm undoped Si spacer layer was grown followed by a second growth interrupt for the deposition of an Sb δ-doped layer ($3\times10^{14}/\mathrm{cm}^2$). The final layers were a spacer layer of 70 nm of undoped Si followed by 30 nm of Sb-doped ($>10^{20}/\mathrm{cm}^3$) Si for the top Ohmic contact. The Si growth rate was 0.1 nm/s, with the exception of the δ-doped regions during which the Si flux was shuttered. Prior to device fabrication, portions of the samples were annealed to determine if postgrowth anneal improved the device characteristics, analogous to our previous RITD work.[14–16] Rapid thermal anneal (RTA) was employed using temperatures of 600, 650, or 700 °C for a period of 1 min.

Atomic profiles were obtained by secondary ion mass spectrometry (SIMS) using a high-performance magnetic sector secondary ion mass spectrometer. The net impact energy of the primary beam, 3 keV O_2^+, was selected in order to minimize profile broadening by ion-beam mixing. Depth scales were obtained from stylus profilometry ($\pm3\%$ uncertainty). The atomic carrier concentrations of B and Sb were calibrated with implant standards ($\pm10\%$ uncertainty). The electrically active portion of the RITD is the region which includes the n^+ layer, the p^+ layer, and the undoped spacer between them. This region is presented in Fig. 2, for the as-grown sample (solid lines) and the sample which underwent RTA for 1 min at 700 °C (dashed lines). Some of the width observed in the doping profiles is due to ion-beam mixing during the SIMS measurement. The portion of the dopant profiles extending into the sample are more affected by the SIMS measurement. It is observed that the B δ-doped profile was affected by the RTA. The half width at half maximum, toward the surface, increased from 3 to 5 nm. There was a corresponding reduction in the peak B concentration from 3.6×10^{20} to $2.5\times10^{20}/\mathrm{cm}^3$. The differences observed between the as-grown and annealed Sb δ-doped profiles are within the mutual uncertainties of the SIMS measurements. Based on the atomic distributions obtained by SIMS, the band diagrams for the RITD, as-grown, and after RTA for 1 min at 700 °C, were generated by solving the effective-mass Schrödinger equation and corresponding quantum charge for each band and iterating to convergence with Poisson's equation. It was observed that, after anneal, the tunnel region becomes slightly wider due to the B diffusion. The current–voltage ($I-V$) curves were calculated with a two-band model using the light electron mass of $0.19\ m_0$ and the indirect band gap of 1.12 eV. While the direct tunneling two-band model is not the correct physics for Si, it should predict the correct trends in the magnitude of the current for different junction potentials. These calculations show the current being reduced after RTA, which is consistent with the wider tunnel region, but is inconsistent with the experimental data, as will be shown.

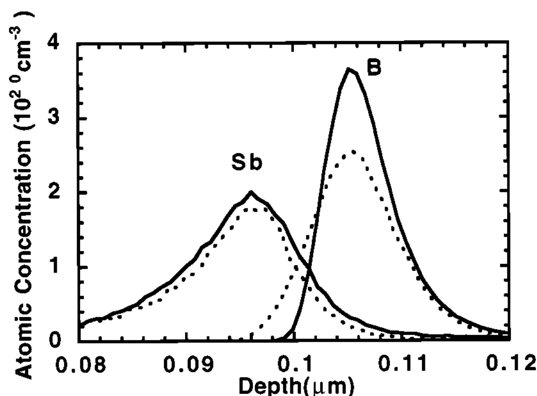

FIG. 2. SIMS atomic profiles of the Si RITD, as grown and after a postgrowth anneal of 700 °C for 1 min. The region of the device, including the δ-doped layers and the intrinsic Si spacer, has been magnified. A linear scale was used to emphasize the effects of the anneal. The as-grown sample is shown with solid lines. The sample annealed at 700 °C is shown with dashed lines.

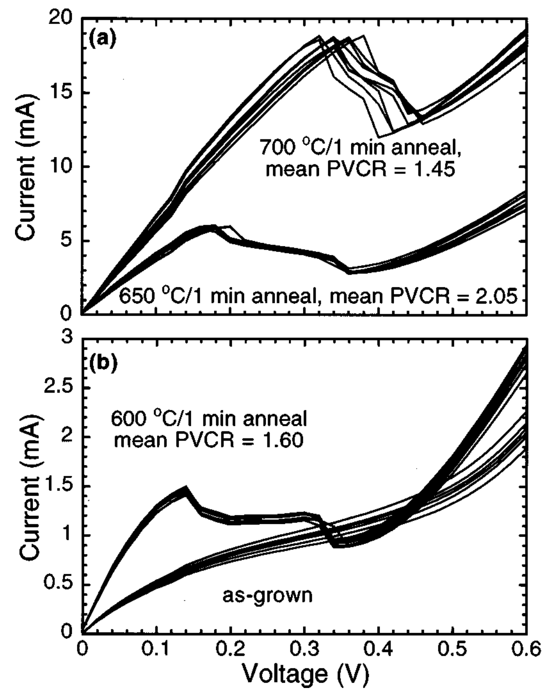

FIG. 3. $I-V$ characteristics for seven adjacent devices after the specified anneal. All measurements are on 18-μm-diam diodes and were taken at room temperature. The results are shown on two graphs because of the increased currents after the anneal.

The fabrication process for the RITDs has been previously described.[14] Room-temperature $I-V$ curves were measured from the top of the mesa to the backside Al contact. $I-V$ measurements for seven adjacent devices, having a diameter of 18 μm, for the as-grown samples and for each anneal condition, are presented in Fig. 3. It is seen that the as-grown RITDs do not exhibit NDR, but have $I-V$ charac-

teristics of backwards diodes. NDR was observed following a postgrowth RTA between 600 and 700 °C. In the following discussion we focus on four characteristics of these curves: PVCR, the voltage V_p at which the relative maximum in the current I_p occurred, and the peak current density J_p.

The average PVCR was 1.60, 2.05, and 1.45 after a 1 min RTA of 600, 650, and 700 °C, respectively. These room-temperature values are significantly larger than reported PVCR values for epitaxial Si tunnel diodes at any temperature.[5–14,17] It is observed that V_p shifted to larger values with higher anneal temperature. The plot of V_p vs I_p was linear. The intrinsic series resistance obtained from the slope of the curve had a value of 12.2 Ω. The intrinsic peak voltage of the diodes was obtained from the intercept and had a value of 117 mV. This agreed well with the predicted value of 90 mV from the model. The peak current density increased with the anneal temperature from 5.7×10^2 A/cm^2 after the 600 °C/1 min anneal to 7.3×10^3 A/cm^2 after the 700 °C/1 min anneal. It is not clear why the device characteristics improved with anneal temperature. The diffusion of the B, observed by SIMS after the 700 °C RTA, widened the tunnel junction by compensating the *n*-type dopants and should result in a lower peak tunnel current. The simplest explanation for device improvement is the reduction of defects and increased activation of dopants in the quantum wells by the anneal. In the band-structure diagram we assumed complete activation at the growth temperature based on prior work on highly doped thick layers. This assumption may not be valid for the δ-doped layers and will be investigated further.

In summary, we have reported on the growth and characterization of Si RITD, which have significantly improved PVCR (>2) compared to previously reported epitaxial Si diodes. The growth was accomplished using low-temperature (320 °C) epitaxy to minimize the segregation of the dopants, which, in turn, permitted a very high concentration of *p* and *n* dopants in the quantum wells. A postgrowth RTA between 600 and 700 °C was required to observe NDR. The low growth and anneal temperatures and the thin epitaxial thickness requirement make these device suitable for CMOS and HBT integration.

This work was supported by the Office of Naval Research, National Science Foundation, and Defense Advance Research Projects Agency. The authors thank Lt. Col. Gernot Pomrenke for his encouragement throughout the project.

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