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Investigation of the Interface Region Produced by Molecular Beam Epitaxial Regrowth

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The interface region generated by molecular beam epitaxial regrowth has been studied in detail. Regrowth was carried out on epitaxial GaAs after a variety of realistic device processing steps. Combinations of wet chemical etching and ion milling with and without annealing were used with the objective of establishing the best procedure for integrated technologies during regrowth. Capacitance voltage measurements showed perturbations in the carrier profile corresponding to depletion and accumulation regions at the interface which are directly related to interface states at and around the regrowth interface. The measured concentration of the interface states are in the range 1.2×10^{10} to 7.05×10^{11} cm^{-2}. The former is one of the lowest reported till date. The concentration of deep traps in the regrown layer and interface, observed by deep level transient spectroscopy, is much lower than the interface state density. Their contribution to carrier perturbation is insignificant, except in one case where an electron trap has a rather high concentration. Results of secondary ion mass spectroscopy indicate that the presence of carbon at the regrown interface is not principally responsible for creating the high resistivity interface region. Our data favor the concept of a disordered region created at the interface during regrowth. Interface state density and trap densities are much larger in the wet chemically etched samples, which is further supported by the results of temporal photoresponse measurements on junction photodiodes. The overall characteristics of the dry etched regrowth interfaces seem to be much more promising than the wet chemical etched ones.

Key words: Molecular beam epitaxy, Regrowth, GaAs

I. INTRODUCTION

Molecular beam epitaxy (MBE) has emerged as an extremely powerful technique for device fabrication with III-V compound semiconductors. MBE provides excellent control of thickness and doping profiles, thereby meeting the requirements of high speed digital, microwave, optoelectronic and integrated optoelectronic devices. Several types of advanced device concepts such as quantum interference devices[1] or optoelectronic integrated devices[2,3] may be realized with controlled epitaxial regrowth. Molecular beam epitaxial regrowth has already been used successfully for the fabrication of optoelectronic devices like multiquantum well modulators[3] and GaAs/AlGaAs lasers.[4]

The technology of liquid phase epitaxial (LPE) regrowth of GaAs is widely used, but MBE regrowth of GaAs is not well understood or established. The physical anomalies occurring at the MBE regrown interfaces are only recently being elucidated and need careful investigations for their elimination. Early investigations[5-7] have shown that standard MBE substrate preparation procedures consisting of chemical etching of substrates followed by vacuum desorption of oxides before growth leads to a free carrier loss at the substrate-epilayer interface. Similar depletion of carriers is observed when MBE regrowth is carried out, either after interruption of growth in the growth chamber, or after the grown layer has been exposed to environments outside the growth chamber. Carrier-depletion is accompanied with anomalous C-V carrier profiles which show depletion, accumulation, or both at the interface, which are apparently not related to any intentional doping. As a result, a highly resistive layer forms at the regrown interface. The mechanisms for such anomalous behavior are not fully understood although various models and explanations have been proposed. Trap formation or compensation by arsenic vacancies, site change of silicon atoms leading to compensation, absorption of impurities like carbon or oxygen at the interface leading to negatively charged levels, deep electron traps and/or ionized deep levels, have been separately or collectively thought to be responsible for the depleted interface region.[6,7,10] It has also been suggested[6,8,9,18] that the high resistivity layer may arise from a disordered region at the interface leading to interface states and deep levels.

Several techniques have been used to partially or totally eliminate the high resistive layer at the regrown interface. Counter doping of the interface

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during regrowth,[7] thermal oxidation of the interface region and desorption of the oxide prior to regrowth,[11] and evaporation of gallium atoms[12] at a temperature above 700° C before regrowth are some of the techniques that have been employed. Passivation of the GaAs layers before bringing them out of the growth chamber by arsenic,[13,14] indium arsenide[15] or antimony,[16] and desorbing the passivating layer prior to regrowth have also been found to inhibit the formation of the resistive region in spite of the layers being exposed to air and deionized water.

In most of the previous work described above, MBE regrowth of GaAs has not been studied when the interface is exposed to conditions such as those encountered during actual device fabrication. In this paper we present results of a detailed investigation of regrown interfaces of GaAs formed by MBE. The surfaces, prior to regrowth, have been dry etched or chemically etched, as are necessary for device fabrication in advanced integrated optoelectronics. The aim of such investigations is to understand the regrown interface and to establish the best procedures for advanced device fabrication using regrowth.

II. EXPERIMENTAL TECHNIQUES

All MBE growth and regrowth were done in a Varian Gen II MBE system. The first step was to grow 1.5 μm n-GaAs doped with silicon (1×10^{16} cm^{-3}) on a silicon doped n^+[100] GaAs substrate. The substrates were solvent degreased, etched in $5H_2SO_4:1H_2O_2:1H_2O$ for 90 sec at 60° C and finally etched in $1HCl:1H_2O$ before mounting them on the molybdenum holders for epitaxy. Before commencing growth, the residual oxides on the substrate were desorbed at 630° C and an arsenic-stabilized surface was established by in-situ monitoring of the electron diffraction pattern. Growth was carried out at 610° C at a rate of 0.8 μm/h with an arsenic to gallium flux ratio of 18:1.

After the first growth the GaAs layer was removed from the growth chamber and separate pieces of it were subjected to the processes listed in Table I, as a simulation of different device fabrication steps. The processing techniques investigated can be classified into two major groups: 1) wet chemical and dry etching with and without furnace annealing, and 2) etching with and without annealing under an arsenic flux inside the growth chamber before regrowth. The samples were wet-etched for 13 sec in (1:1:5) $H_3PO_4:H_2O_2:H_2O$ (samples A,B) or for 60 sec in $NH_4OH:H_2O_2:H_2O$ (3:1:50) (samples C,D). Dry etching was carried out in a MILLATRON ion milling system (E,F,G) and rapid thermal annealing (RTA) was done in a HEATPULSE 210 unit (E,G). Samples B, D and F were annealed before regrowth inside the MBE growth chamber under an arsenic flux at 610° C for 20 min.

The effect of reducing the temperature and growth rate during regrowth was also studied (G). The etched samples were reinserted into the growth chamber and after the desorption described earlier, a layer ($\cong$1.4 μm) of GaAs was regrown under identical growth conditions.

Gold Schottky barriers were fabricated on the regrown GaAs layers for characterization of the interface by capacitance-voltage (C-V) carrier profiling, Deep Level Transient Spectroscopy (DLTS) and optical measurements. Carrier profiling using the C-V technique was carried out in a HP 4275A LCR meter. DLTS measurements were made with a facility containing a variable-temperature cryostat, a 1MHz BOONTON capacitance meter and a signal analyzer providing the trigger pulses and rate windows.

III. RESULTS AND DISCUSSIONS

a) Capacitance-Voltage Measurements

Typical carrier profiles obtained at room temperature for two types of etched interfaces are shown in Fig. 1. As observed by previous workers,[7-9,11-14] the carrier profiles show a strong depletion around the regrown interfaces and an accumulation region in the form of a spike towards the substrate. Using the model of Kroemer *et al.*,[17] modified suitably for our purposes, the interface state densities presented in Table I were calculated. The imbalance of charge between the apparent carrier profile, as obtained experimentally, and the nominal donor concentration profile obtained from the growth parameters gives the interface states density around the regrowth interface, the observed deep levels being accounted for. It was found that the density of deep levels, characterized in the course of this study, compared to the interface state density was much lower. This rules out the possibility of native defects such as lattice vacancies being totally responsible for the anomalous effects observed at regrown interfaces.

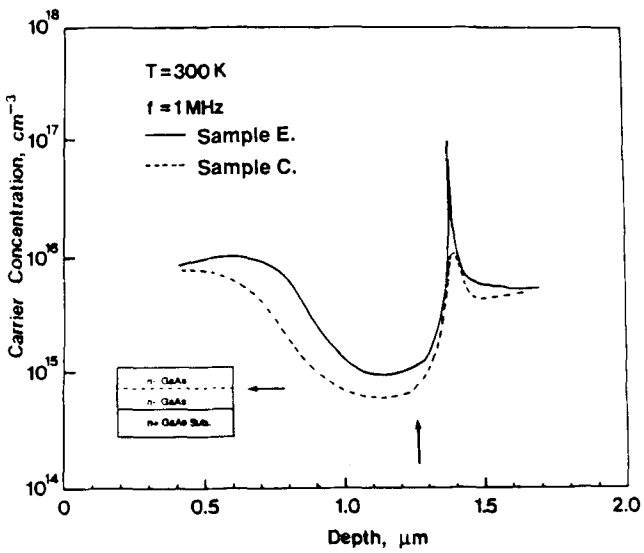


Fig. 1 — Measured carrier concentration profiles in regrown GaAs layers around the growth interface.

Table I. Processing Parameters used before GaAs Regrowth and Interface State Densities Measured in Regrown GaAs Samples.

Sample	Etching Technique	Interface States Density (cm^{-2})
A	$H_3PO_4:H_2O_2:H_2O(1:1:5)$	7.05×10^{11}
B	A + As anneal (20 min)	5.78×10^{11}
C	$NH_4OH:H_2O_2:H_2O(3:1:50)$	6.56×10^{11}
D	C + As anneal (20 min)	5.26×10^{11}
E	Ion Milling + RTA at 900° for 7 sec	1.01×10^{11}
F	Ion Milling + As annealing for 20 min	4.89×10^{11}
G	E + Growth Rate Low/Low T_{sub}	1.20×10^{10}

Figure 2 shows the C^{-2}-V plot for a typical regrown interface. As proposed by Hasegawa *et al.*[8,18] the plot can be divided into three regions a, b, c, which can be interpreted in terms of the band diagrams shown in Fig. 3. Region (a), away from the regrowth interface, shows normal behavior. Carrier depletion is seen in the region (b) due to the notch in the conduction band profile introduced by interface states when the edge of the depletion crosses this region. With increasing reverse bias, when the Fermi level crosses the energy level of the states, release of carriers from these states manifests as a carrier accumulation of region (c) in the plot. When the traps are emptied, normal behavior is restored. Using the model of Hasegawa *et al.*,[8,18] the interface state distribution is calculated from:

$$\frac{dC^{-2}}{dV} = \frac{2}{q(1+B)N_D} \tag{1}$$

$$\text{where} \quad B = \frac{q^2 N_{It}}{\epsilon_s x_w(V)} \chi_i [\chi_w(V) - \chi_i] \tag{2}$$

$$\text{and} \quad E = E_c - qV_n - \frac{q^2 N_D}{2\epsilon_s} (\chi_w(V) - \chi_i)^2 \tag{3}$$

N_{It} is the interface state density, ϵ_s is the semiconductor permittivity x_i, $x_w(V)$ are the depth of the interface and the total depletion width at bias V,

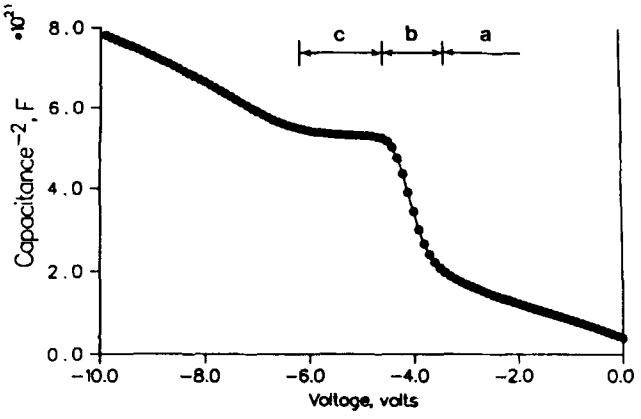


Fig. 2 — Typical C^{-2}-V plot around regrown interface.

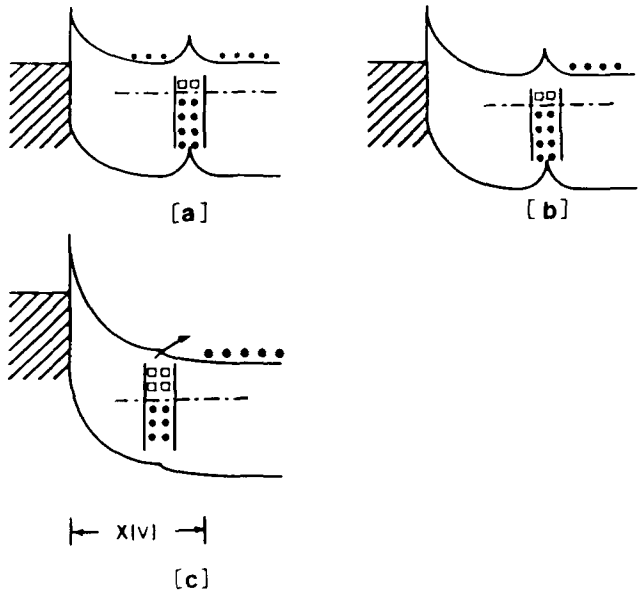


Fig. 3 — Band diagrams showing the behavior of interface states with increase in reverse bias.

respectively, and qV_n is the energy distance between the conduction band and the bulk Fermi level. The interface state distributions are shown in Fig. 4. It may be noted that the point of minimum density is in the range of 0.7–0.8 eV and the density is lowest for sample G. There is one exception to the role of deep level traps. Some samples exhibited an apparently anomalous interface state distribution, as shown for sample D in Fig. 4. A peak in the density is observed at ~0.5 eV for this sample. This energy coincides with the thermal activation energy measured for electron trap M4, to be described later and this trap density is high in samples showing the anomalous behavior of N_{it}.

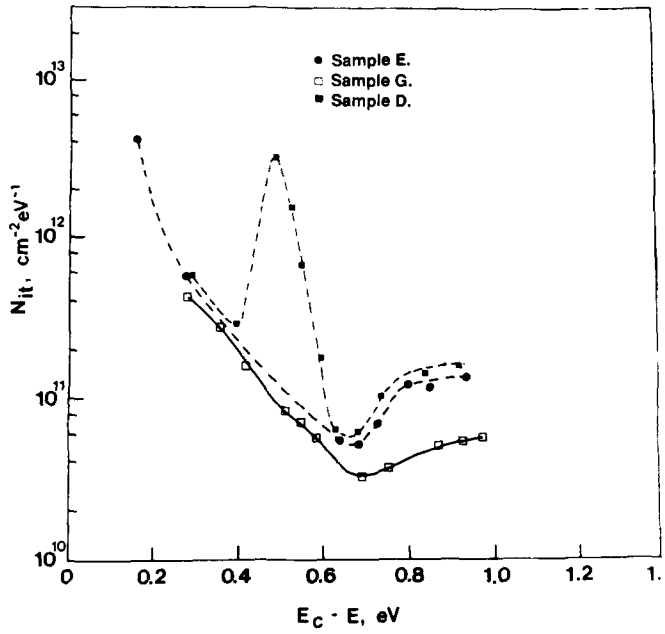


Fig. 4 — Measured interface state distribution at regrown interfaces.

b) Deep Level Transient Spectroscopy

DLTS measurements on the regrown layer and at the interface reveal the electron traps M1, M2, M3, and M4 and M6, which are commonly observed in MBE GaAs.[19-22] The traps (except M2) were also identified in the as grown layer. The maximum concentration of the electron traps are around 10^{13} cm^{-3}. The characteristics of these traps are listed in Table II. From detailed measurements on a number of samples it was found that the electron trap concentrations do not increase at the interface region, but there is an overall increase in the concentration after annealing under arsenic overpressure in the growth chamber to a value of approximately 10^{14} cm^{-3}. In fact, the traps M2 and M6 appear only in arsenic-annealed samples. Figure 5 shows the observed DLTS signal for electron traps identified in different samples for a specific rate window setting. Suggestions regarding the origin of these electron traps are controversial. Lang *et al.*[19] suggested that the traps are related to impurities, which was supported by Blood *et al.*[20] excepting the proposition that M2 is related to defect complexes involving As-vacancies. Observations by Skromme *et al.*[21] strongly suggest that the electron traps are not related to impurities, which is supported by the conclusions of Dhar *et al.*[22] that the traps may be related to gallium vacancies. The increase in electron trap densities after annealing in an arsenic overpressure in our experiments strongly suggests that increased gallium vacancies may be responsible for the formation of these traps.

In addition, two hole traps with activation energies of 0.28 eV and 0.36 eV were observed in the interface regions of the regrown wet chemical etched samples. The concentration of the hole traps increases at the regrowth interface to a value of the order of 1×10^{14} cm^{-3}. It was observed that the density of these hole traps were reduced by an order of magnitude by annealing under arsenic flux in the MBE chamber. Annealing may reduce the density of point defects or complexes in the disordered interface growth region, which may account for the reduction in the trap density. DLTS data of the hole traps in H_3PO_4-etched samples with and without arsenic anneal are shown in Figs. 6 and 7 and the characteristics of the observed traps are summarized in Table II.

Table II. Characteristics of Electron (M) and Hole (H) Traps in As-Grown and Regrown MBE GaAs.

Type of epitaxial layer	Trap Label	ΔE_T (eV)	α_∞ (cm^2)
As-grown GaAs	M1	0.21	1.7×10^{-13}
	M3	0.33	1.0×10^{-14}
	M4	0.52	1.5×10^{-13}
	M6	0.75	2.0×10^{-11}
Regrown GaAs[1]	M2	0.29	
	H1	0.36	2.2×10^{-18}
	H2	0.28	1.5×10^{-18}

[1]These traps were detected in addition to M1, M3, M4 and M6.

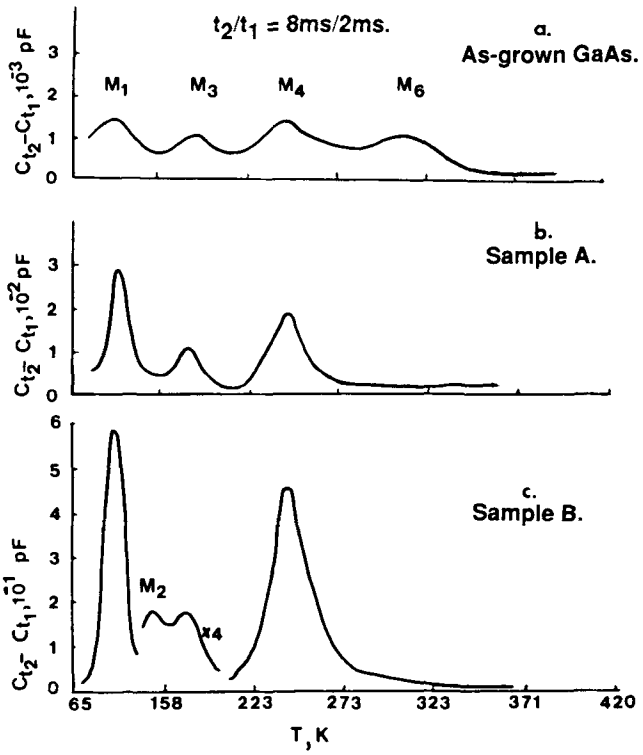


Fig. 5 — Electron traps identified in as-regrown MBE GaAs (a), in regrown GaAs after H_3PO_4 etch (b), and in regrown GaAs after H_3PO_4 etch and annealing under arsenic flux (c).

Early work on regrown interfaces suggest that the depletion of carriers at the interface could be due to incorporation of impurities at the interface and carbon in particular.[6,7,10,14] Secondary Ion Mass Spectroscopy (SIMS) was done on some of the regrown layers and the (SIMS) profiles of carbon in samples with two types of regrown interfaces are shown in Fig. 8. The samples correspond to A and E in Table I. From the SIMS results we see that the concentration of carbon at the interface of E is much higher than that of A. If the depletion of carriers is solely due to the carbon impurities at the interface we should have had much larger depletion in E, but the results are to the contrary. Both, the total trap concentration and interface state density are much lower in E as compared to those in A. Similar depletion-accumulation behavior has also been ob-

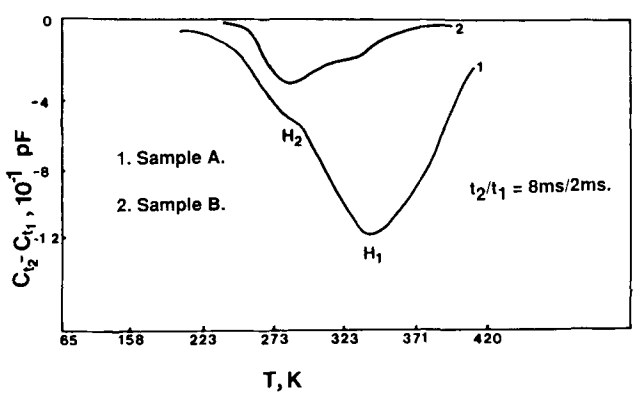


Fig. 6 — Hole traps identified at the regrown interface and their reduction on annealing under arsenic flux prior to regrowth.

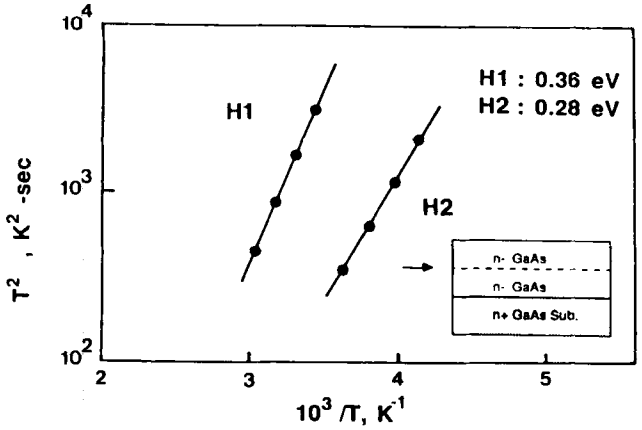


Fig. 7 — Arrhenius plots of the observed hole traps.

served in Be-doped regrown interfaces,[9] which rules out the possibility of Si autocompensation at or near the regrown interface, since Be is always incorporated as acceptors. This leads us to conclude that the depletion of carriers does not originate only from carbon, but may arise from a disordered region formed at the interface during regrowth, as suggested by Hasegawa.[8,18] Accumulation is observed due to the emptying of the interface states with increased reverse bias when the Fermi level crosses the energy levels of the interface states. This is further supported by the experimental evidence that the accumulation is less pronounced in C-V data taken at 77K, where the emission rate of electron and holes from the interface traps is much lower.

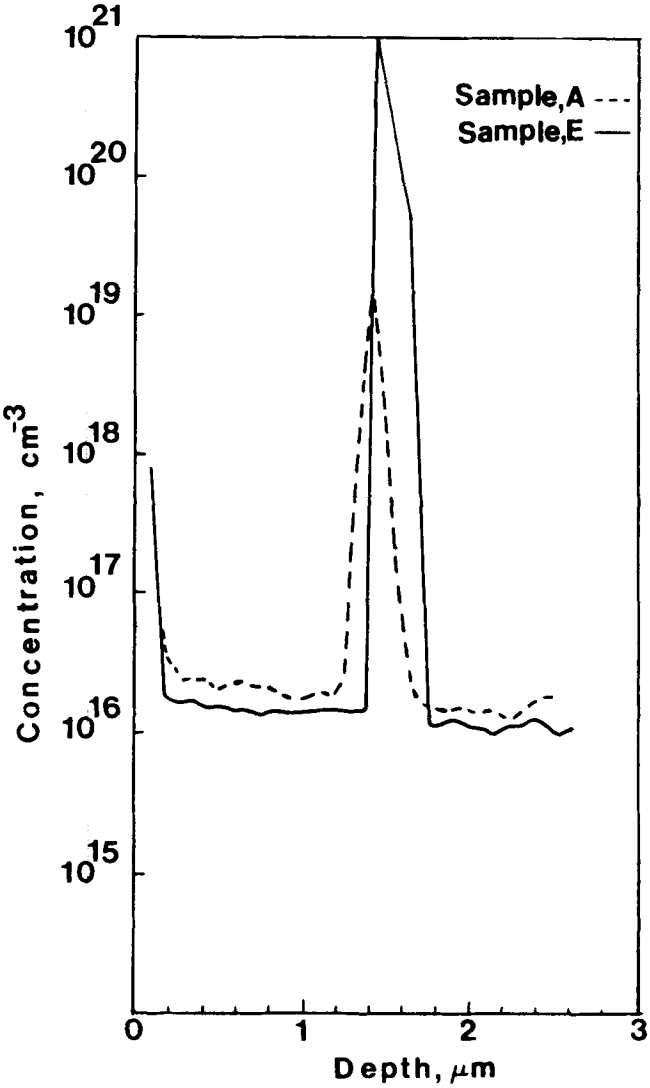


Fig. 8 — Results of secondary ion mass spectroscopy showing carbon concentrations in samples A and E at the regrowth interface.

c) Temporal Photoresponse Characteristics

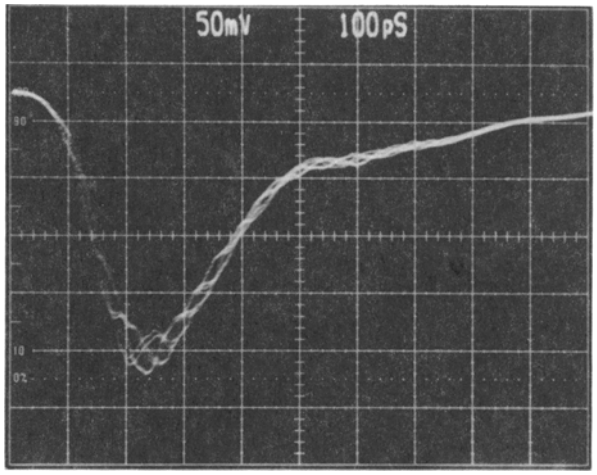
The degradation in the impulse response of photodiodes made on the regrown GaAs layers were investigated. The mesa diodes have an area of 25 μm^2 and a total transit length ~1.5 μm. For these dimensions a homojunction diode has a response speed (FWHM) of ~200 ps. The response characteristics of two regrown diodes are shown in Figs. 9 (a) and (b). It appears that H_3PO_4-etched samples have the largest fall time in the photoresponse characteristics. These samples also have the largest trap density and a large interface state density. It may, therefore, be concluded, with some caution that the long response is a direct manifestation of these defects.

IV. CONCLUSIONS

MBE regrowth of GaAs on epitaxial GaAs has been investigated in detail, with the regrowth surface being exposed to processing conditions as encountered in actual device fabrication. The regrown layers, when characterized by C-V profiling, show an anomalous carrier depletion and accumulation around the regrowth interface. DLTS measurements on the regrown layers reveal a number of deep electron and hole traps at the interface region but their concentration is not high enough to account for the observed carrier depletion. Such depletion is attributed primarily to the large concentration of interface states around the regrowth interface as computed from carrier profiles. An anomaly in the interface state distribution is noticed in some samples. There is a peak around 0.5 eV which corresponds to the energy of the deep level M4.

SIMS data indicate that the depletion of carriers cannot be explained only by the presence of carbon at the interface. These results strongly suggest that the carrier depletion originates mainly from the interface states created by a disordered region during regrowth and the accumulation is observed when carriers are released from these states. This is further supported by the observation that the accumulation almost disappears at 77K.

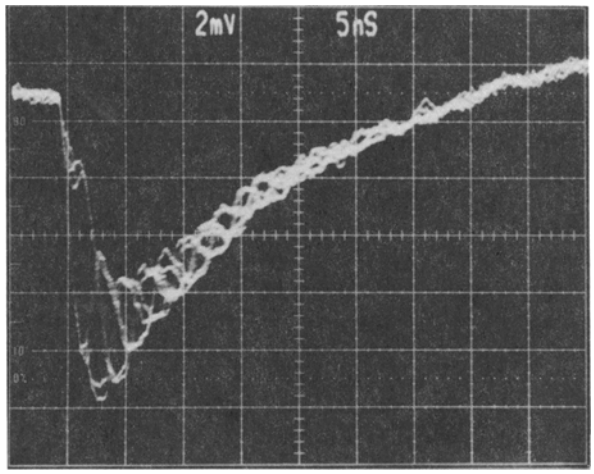
Temporal photoresponse results clearly show that the response time decreases with the decrease in the concentration of the interface states. Concentrations of deep traps and interface states are much lower in the dry etched interfaces as compared to the wet chemical etched interfaces. The difference is more pronounced for the sample with a lower



Sample E.

Fall Time = 580 ps

(a)



Sample B.

Fall Time = 25 ns

(b)

Fig. 9 — Temporal photoresponse characteristics of photodiodes made on samples E and B.

growth temperature. It seems that a lower regrowth temperature reduces the propagation of defects from the regrowth interface.

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